MODEL 8132

TIME CODE READER

INSTRUCTION MANUAL

LEPHONE NUMBERS

AUSTRON

AUSTRON INC. P.O. BOX 14766 - EXIT 248, N. IH 35, AUSTIN, TEXAS 78761 (512) 251-2341 TWX 910/874-1356

MASTER COPY

MODEL 8132
TIME CODE READER
INSTRUCTION MANUAL

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REVISION C

NOTICE:

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ADDRESSES AND TELEPHONE NUMBERS

WARRANTY

AUSTRON, INC., of Austin, Texas, warrants, for one year after delivery, to the original purchaser of any product manufactured by AUSTRON, that same shall be free of defects in material and workmanship. Obligation under this warranty shall be limited to repair or replacement, at AUSTRON's discretion, of any product or part thereof which has been returned by the original purchaser with transportation prepaid, and upon examination by AUSTRON, is found to be defective. AUSTRON assumes no reponsibility for loss or damage to equipment being returned for repair or replacement under the terms of this warranty.

For this warranty to be effective, the purchaser agrees that the equipment will be properly installed and maintained. Equipment which, upon examination by AUSTRON, requires repair or replacement of parts thereof as a result of improper installation, misuse, unauthorized alterations or repairs, or user negligence, such repairs or replacement of parts thereof will be made at cost.

AUSTRON makes no representation or warranty of any kind, either expressed or implied, with respect to equipment operation and procedures. Any action that the user may take in reliance upon the operation or accuracy of this equipment shall be taken solely upon the user's own responsibility and risk.

AUSTRON shall not be liable for consequential damages to purchaser, user, or any others resulting from the possession or use of this equipment.

Prior to return of a product under terms of this warranty, AUSTRON, INC., Austin, Texas, is to be notified. Notification is to include the Model Number and Serial Number of the product and full details of the problem.

STANDARD OPTIONS

Standard options installed in your unit are checked below. Circuit descriptions for these options are provided in Chapter Six. Special modifications, when included, are described in Chapter Seven.

OPTION	DESCRIPTION
A12A	Slow Code, Type A
A12B	Slow Code, Type B
A16C	Control Bit Translation
A16D	Control Bit Translation & LED Display
A21	Computer Read Command/Data Freeze
B17	Flywheel Oscillator
C11	IRIG A (10 KHz) Code
C12B	Binary Seconds
C17	NASA 28-Bit (100 Hz) Code
C18	NASA 36-Bit (1 KHz) Code
C26	XR3 (250 Hz) Code
C26A	XR3 (1 KHz) Code
C31	IRIG G (100 KHz) Code
C40	IRIG A, B, C (100 Hz), C (1 KHz), E (100 Hz), E (1 KHz) Switch Selectable
C41	IRIG A, B Switch Selectable
C47	XR3 (250 Hz/1 KHz) Switch Selectable
C48	IRIG H (100 Hz)
C48A	IRIG H (1 KHz)
D14	Group Parallel BCD Outputs with Storage
D15	Parallel BCD Output
E13	Days/ID Number
E14	Parallel BCD Output, Milliseconds
L12	48 Hz to 440 Hz Operation
L13	AC/DC Power Supply
P11	Remote Mode Control
P14	Remote Code Select (Option C40)
P20	Remote Slow Code Rate Select
S13	Analog Filters, Local
S14	Analog Filters, Remote
	Special Modifications (See Chapter Seven)

TABLE OF CONTENTS

		Page
CHAPTER 1 - GENERAL DESCRIPTION		
1.1	Introduction	1-1
1.2	Specifications	1-2
1.2.1	Display	1-2
1.2.2	Code Format	1-2
1.2.3	Inputs	1-2
1.2.4	Outputs	1-2
1.2.5	Environment	1-2
1.2.6	Power	1-2
1.2.7	Package	1-2
CHAPTER 2 - INSTALLATION		
2.1	Initial Inspection	2-1
2.2	Storage and Reshipment	2-1
2.3	Power and Cooling Requirements	2-2
2.4	Initial Adjustment	2-2
2.5	Installation	2-2
CHAPTER 3 - OPERATION		
3.1	General	3-1
3.2	Controls, Indicators and Connectors	3-1
3.2.1	Front Panel	3-1
3.2.2	Rear Panel	3-1
CHAPTER 4 - MAINTENANCE AND CALIBRATION		
4.1	Factory Service	4-1
4.2	Routine Maintenance	4-1
4.3	Printed-Circuit Board Repair	4-2
4.4	Operational Test and Calibration Procedure.	4-3
4.4.1	Recommended Test Equipment	4-3
4.4.2	Power Supply	4-4
4.4.3	Power Supply Regulator	4-4
4.4.4	AGC & Cycle Detector	4-4
4.4.5	Reverse Operation	4-6
4.4.6	Sensitivity	4-7
4.4.7	Frequency Response	4-7
4.4.8	Error Bypass	4-7
4.4.9	General Checkout	4-7
CHAPTER 5 - FUNCTIONAL DESCRIPTION		
5.1	General	5-1
5.1.1	Reference Designations	5-1
5.1.2	Logic Functions	5-2

TABLE OF CONTENTS (CON'T)

CHAPTER 5 - FUNCTIONAL DESCRIPTION (CON'T)

		PAGE
5.2	Function	5-4
5.2.1	AGC/Cycle Detector	5-4
5.2.2	Reader Logic	5-4
5.2.3	Minor Counter	5-5
5.2.4	TOD Accumulator	5-5
5.2.5	Code Generator	5-5
5.2.6	Preset and Error Bypass	5-5
5.2.7	FWD-REV Control	5-5
7-06103402	Model 8132 Time Code Reader (IRIG B)	
	Block Diagram	5-7
	Final Assembly Parts List	5-8
021535-7-3	20-Bit Buffer Circuit Description	5-10
	Schematic	5-11
	Assembly	5-12
	Parts List	5-13
021543-7-3	Time-of-Day Accumulator Circuit	
	Description	5-14
	Schematic	5-15
	Assembly	5-16
	Parts List	5-17
021554-7-1	IRIG DC Code Generator Circuit	
	Description	5-18
	Timing Diagram (Sheet 1 of 2)	5-20
	Timing Diagram (Sheet 2 of 2)	5-21
	Schematic	5-22
	Assembly	5-23
	Parts List	5-24
021569-7-1	AGC & Cycle Detector Circuit	
	Description	5-25
	Schematic	5-27
	Assembly	5-28
	Parts List	5-29
021588-7-3	Reader Logic Circuit Description	5-31
	Schematic	5-33
	Assembly	5-34
	Parts List	5-35
021625-7-1	FWD/REV Control Circuit Description	5-36
	Schematic	5-37
	Assembly	5-38
	Parts List	5-39

CHAPTER 5 - FUNCTIONAL DESCRIPTIONS (CON'T) PAGE

021632-7-2 Minor Counter Circuit Description 5-39
Schematic 5-41
Assembly 5-42
Parts List 5-43

7-05153802 Preset & Error Bypass Description 5-44
Schematic 5-46
Assembly 5-47
Parts List 5-48

041810-7-9 Power Supply Circuit Description 5-49
Schematic 5-51
Assembly 5-52
Parts List 5-53
Power Supply Regulator Board Assembly 5-54
Parts List 5-55

041945-7-2 Display Assembly Circuit Description 5-58
Schematic 5-59
Assembly 5-60
Parts List 5-61
Display Board Assembly #041766-4-1 5-62
Display Driver Assembly #041772-4-1 5-63
Parts Lists 5-64

CHAPTER 6 - STANDARD OPTIONS

6.1 General 6-1
Days/ID Option E13 . . . . . 6-E13-1
Parts List 6-E13-2

021632-7-1 Days Accumulator Circuit Description 6-E13-3
Schematic 6-E13-4
Assembly 6-E13-5
Parts List 6-E13-6

Parallel BCD Milliseconds Option E14 . . . . . 6-E14-1
Parts List 6-E14-2

CHAPTER 7 - SPECIAL MODIFICATIONS

7.1 General 7-1

LIST OF TABLES

Table 4.1 Test Equipment for Model 8132 4-3
4.2 Power Supply Regulator Voltage Adjustments 4-4
5.1 Reference Desgination 5-1
5.2 Circuit Description Index Information 5-7

TABLE OF CONTENTS (CON'T)

OPTIONAL CODES & CODE FORMATS

IRIG Time Code 1-3
Slow Code - Types "A" & "B" 1-4
AMR Time Code 1-5
XR3 Time Code 1-5
NASA Time Code 1-6

LIST OF FIGURES

Figure 2.1 3-½" Full Rack Assembly #039968-4-5 2-3
4.1 AGC Level Adjustment 4-5
4.2 Cycle Detector Adjustment 4-5
4.3 Lower Large Cycle Adjustment 4-5

CHAPTER ONE

GENERAL DESCRIPTION

1.1 INTRODUCTION

The Model 8132 Time Code Reader decodes an incoming serial modulated time code. Time information stripped from the input code is displayed and fed, in parallel BCD form, to a rear panel connector. The Time Code Reader incorporates extended range AGC, error bypass, and digital filtering for reliable decoding of the incoming time code.

The basic unit reads an IRIG B time code on a 1 KHz carrier. Time is displayed in hours, minutes and seconds. Four pulse rates (1 pps, 10 pps, 100 pps and 1 Kpps) are supplied as outputs.

Other time codes from the IRIG, NASA and XR3 code families may be substituted for IRIG B as options. The unit can be expanded to include Days/ID Number and to provide parallel BCD outputs representing Days/ID and/or Milliseconds. Other options are also available. (Refer to the standard option list at the front of this manual.)

The Model 8132 is constructed with highly reliable semiconductors and monolithic IC's assembled on printed-circuit, plug-in modules for ease of maintenance.

1.2 SPECIFICATIONS

1.2.1 Display

A 6-digit, in-line, in-plane display indicates time-of-day in hours, minutes and seconds. Day option adds 3-digits. Numeral height is 0.55" (14mm). Colons are provided between seconds and minutes, minutes and hours, and hours and days (when the Days/ID Option is included).

1.2.2 Code Format

IRIG B format, in terms of BCD hours, minutes and seconds (Days/ID optional). Other IRIG, NASA or XR3 code formats are available as options.

1.2.3 Inputs

UPDATE INHIBIT: A +5 V level (or open circuit) enables update. A ground condition delays update. Update may be delayed up to 0.5 ms without losing a count. Via rear panel connector, Amphenol 57-40360.

MODULATED CODE, EXTERNAL: The input modulated code, via a rear panel BNC connector, may have a carrier frequency from 30 Hz to greater than 500 KHz, input levels from 50 mV to 50 V peak-to-peak, and modulation ratios from 2:1 to 6:1. Input impedance is 100 KΩ minimum.

1.2.4 Outputs (Outputs are short-circuit-proof to ground)

PULSE RATES: Simultaneous rates of 1 pps, 10 pps, 100 pps, and 1000 pps are provided with leading edge "on time." Levels are 0 to +5 V (nominal) from a 6 KΩ source (DTL). Connector is rear panel Amphenol 57-40360.

PARALLEL BCD OUTPUTS: Updated time is provided as 24 parallel BCD bits (20 active) representing hours, minutes and seconds. Days/ID option adds 12 bits. Connector is rear panel Amphenol 57-40500.

Code:	8-4-2-1.
Logic:	Binary "1" = 5 ±0.5 volts, behind 6 KΩ. Binary "0" = 0 ±0.5 volts, 12 mA sink.

1.2.5 Environment

Operating:	0°C to +60°C at up to 95% relative humidity.
Storage:	-55°C to +85°C.

1.2.6 Power

115/230 V ±10%, 48 to 62 Hz at less than 60 watts.

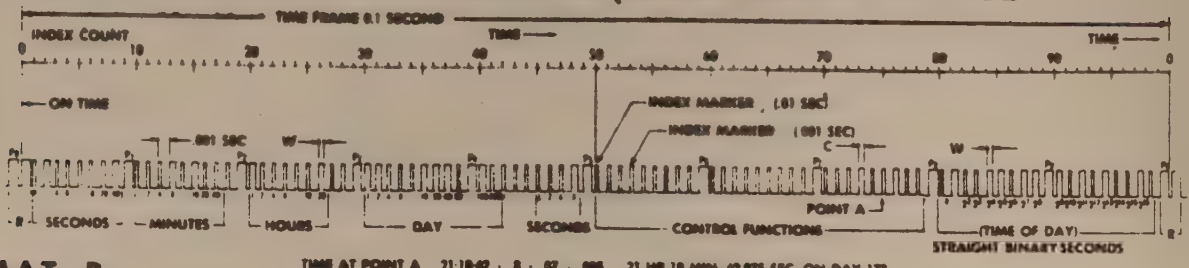
1.2.7 Package

3-½" (8.9 cm) high by 19" wide by 17" (43.1 cm) deep. Removable rack flanges. Chassis drilled for Jonathan 120 QD series slides. Weight approximately 25 lbs (11 kg) net, 35 lbs (16 kg) shipping.

FIGURE 1.1 IRIG TIME CODE FORMATS

FORMAT A

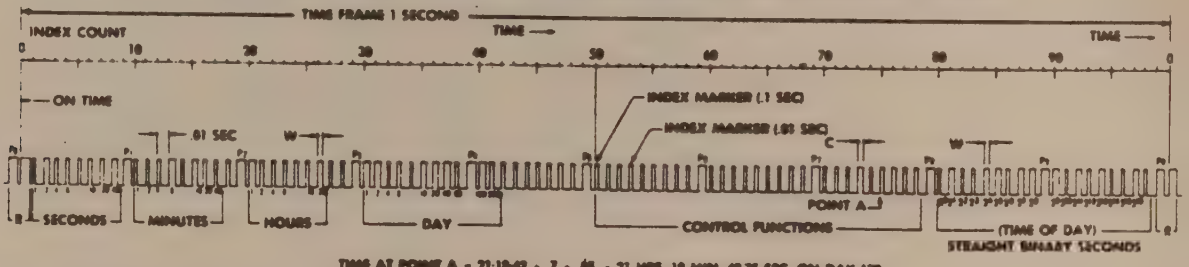
1000-PPS, 34-BIT BCD TIME-OF-YEAR/17-BIT BINARY TIME-OF-DAY CODE



TIME AT POINT A 21:18:42 . 8 . 07 . .085 21 HR. 18 MIN. 42.875 SEC. ON DAY 173

FORMAT B

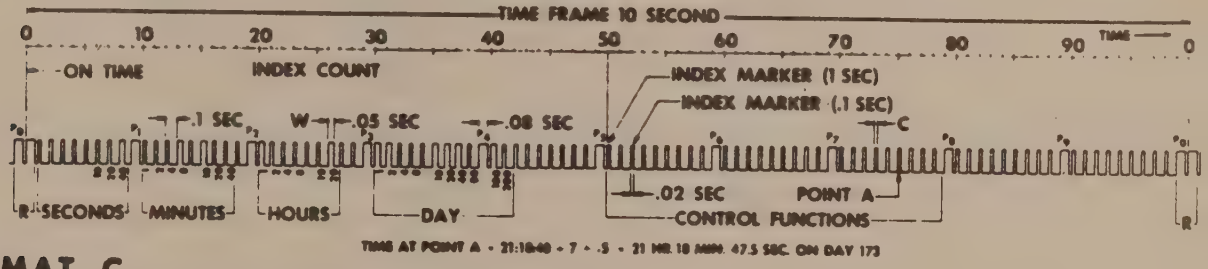
100-PPS, 30-BIT BCD TIME-OF-YEAR/17-BIT BINARY TIME-OF-DAY CODE



TIME AT POINT A - 21:18:42 . 7 . .68 . 21 HRS. 18 MIN. 42.75 SEC. ON DAY 173

FORMAT E

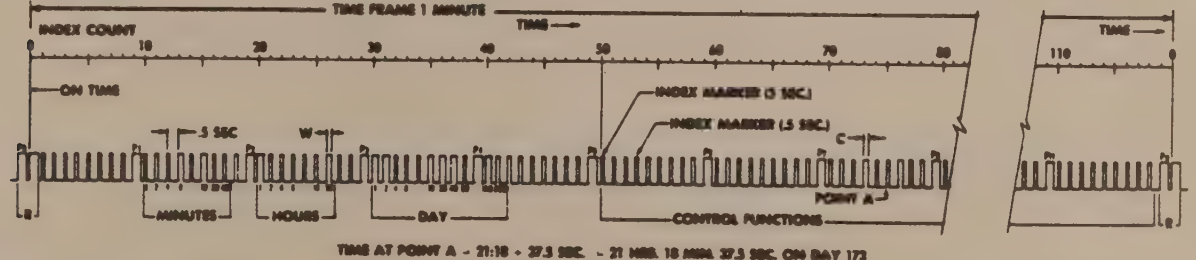
10-PPS, 26-BIT BCD TIME-OF-YEAR CODE



TIME AT POINT A - 21:18:40 . 7 . .5 . 21 HR. 18 MIN. 47.5 SEC. ON DAY 173

FORMAT C

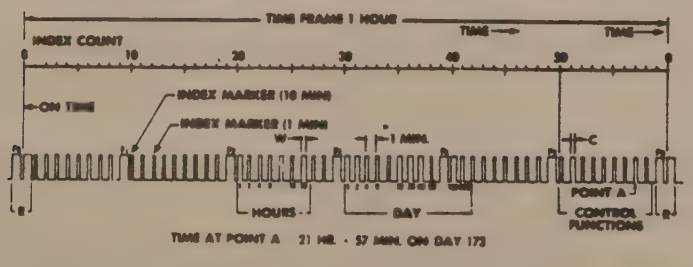
2-PPS, 23-BIT BCD TIME-OF-YEAR CODE



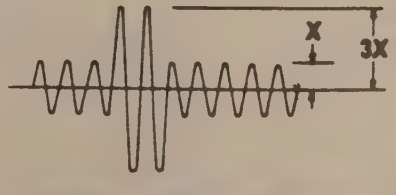
TIME AT POINT A - 21:18 . 37.5 SEC. - 21 HRS. 18 MIN. 37.5 SEC. ON DAY 173

FORMAT D

1-PPM, 16-BIT BCD TIME-OF-YEAR CODE

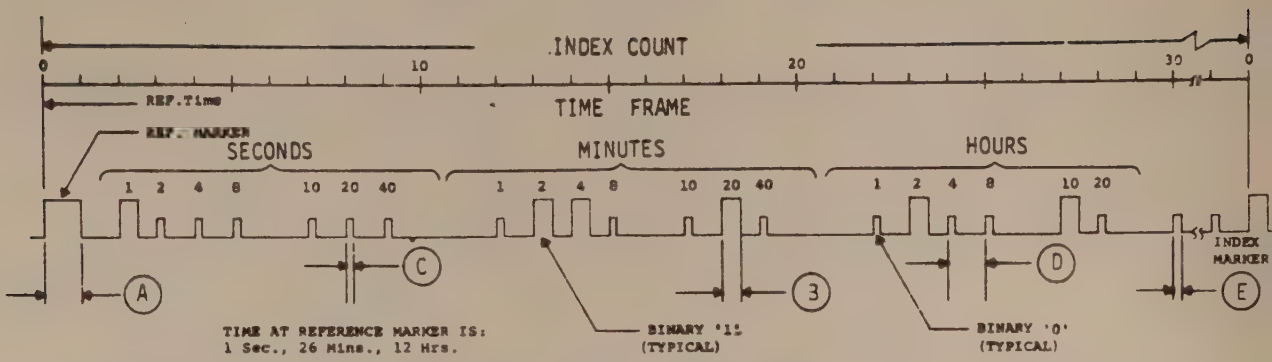


TIME AT POINT A 21 HR. . 57 MIN. ON DAY 173



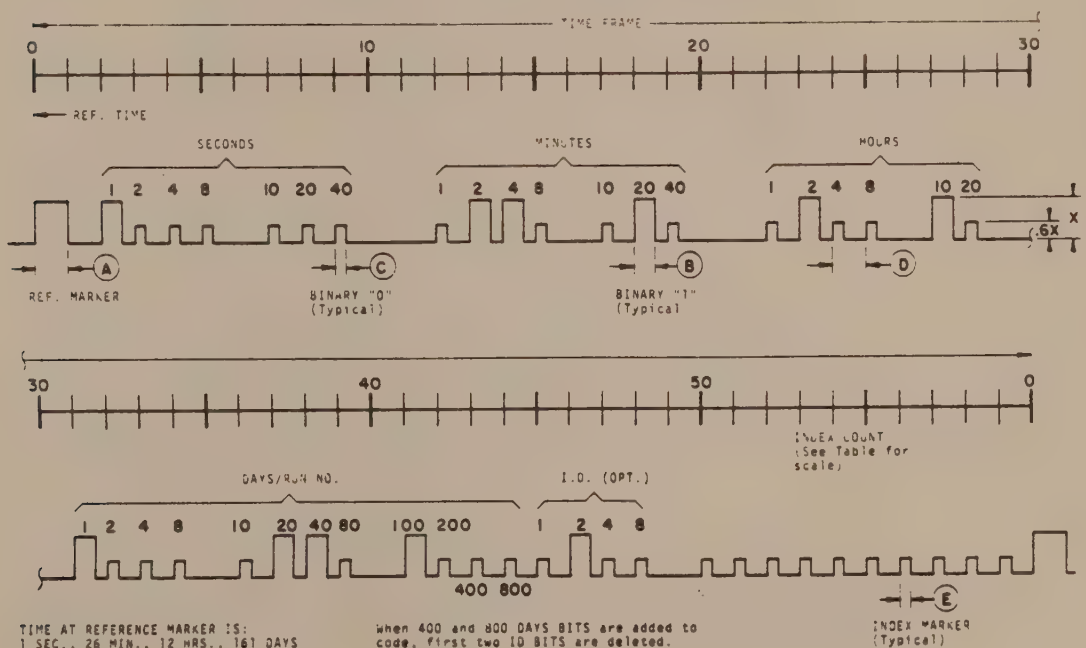
TYPICAL MODULATED SIGNAL

FIGURE 1.2 SLOW CODE - TYPE 'A'



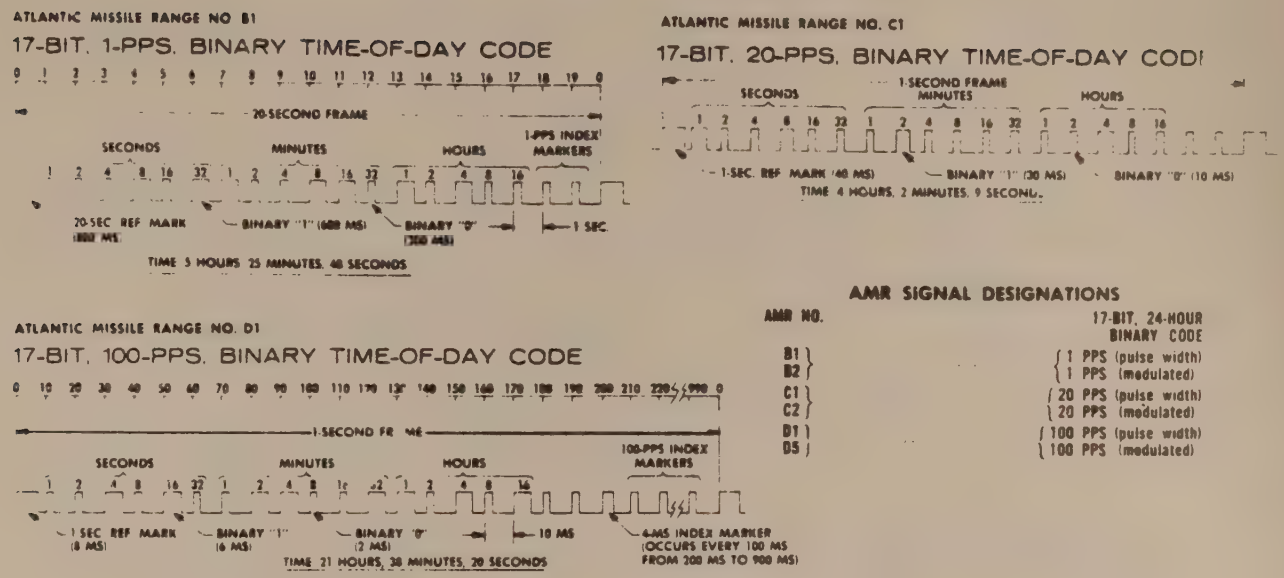
	RATE	TIME FRAME	D-PERIOD	A-WIDTH OF REF. MARKER	B-WIDTH OF BINARY ONE	C-WIDTH OF BINARY ZERO	E-WIDTH OF INDEX MARKER	NO. OF PULSES IN TIME FRAME
1	50 pps	1 Sec.	20 ms	20 ms	10 ms	4 ms	4 ms	50
2	10 pps	5 Secs.	100 ms	100 ms	50 ms	20 ms	20 ms	50
3	5 pps	10 Secs.	200 ms	200 ms	100 ms	40 ms	40 ms	50
4	1 pps	30 Secs.	1 Sec	1 Sec.	500 ms	200 ms	200 ms	30
5	1 2 pps	60 Secs	2 Secs.	2 Secs.	1 Sec.	400 ms	400 ms	30
6	1 10 pps	5 Mins.	10 Secs.	10 Secs.	5 Secs.	2 Secs.	2 Secs.	30
7	1 20 pps	10 Mins.	20 Secs.	20 Secs.	10 Secs.	4 Secs.	4 Secs.	30
8	1 ppm	30 Mins.	1 Min.	1 Min.	30 Secs.	12 Secs.	12 Secs.	30
9	1 2 ppm	60 Mins.	2 Mins.	2 Mins.	1 Min.	24 Secs.	24 Secs.	30

FIGURE 1.3 SLOW CODE - TYPE 'B'



Pulse Rate	Time Frame	D-Period	A-Width	B-Width	C-Width	E-Width	Number of Pulses in Time Frame
1. 50	1 SEC	20 ms	20 ms	10 ms	4 ms	4 ms	50
2. 10	5 SEC	100 ms	100 ms	50 ms	20 ms	20 ms	50
3. 5	10 SEC	200 ms	200 ms	100 ms	40 ms	40 ms	50
4. 2	30 SEC	1/2 SEC	1/2 SEC	250 ms	100 ms	100 ms	60
5 1	60 SEC	1 SEC	1 SEC	1/2 SEC	200 ms	200 ms	60
6 1/2	5 MIN	5 SEC	5 SEC	2-1/2 SEC	1 SEC	1 SEC	60
7 1/10	10 MIN	10 SEC	10 SEC	5 SEC	2 SEC	2 SEC	60
8. 2 ppm	30 MIN	30 SEC	30 SEC	10 SEC	6 SEC	6 SEC	60
9 1 ppm	60 MIN	60 SEC	60 SEC	30 SEC	12 SEC	12 SEC	60

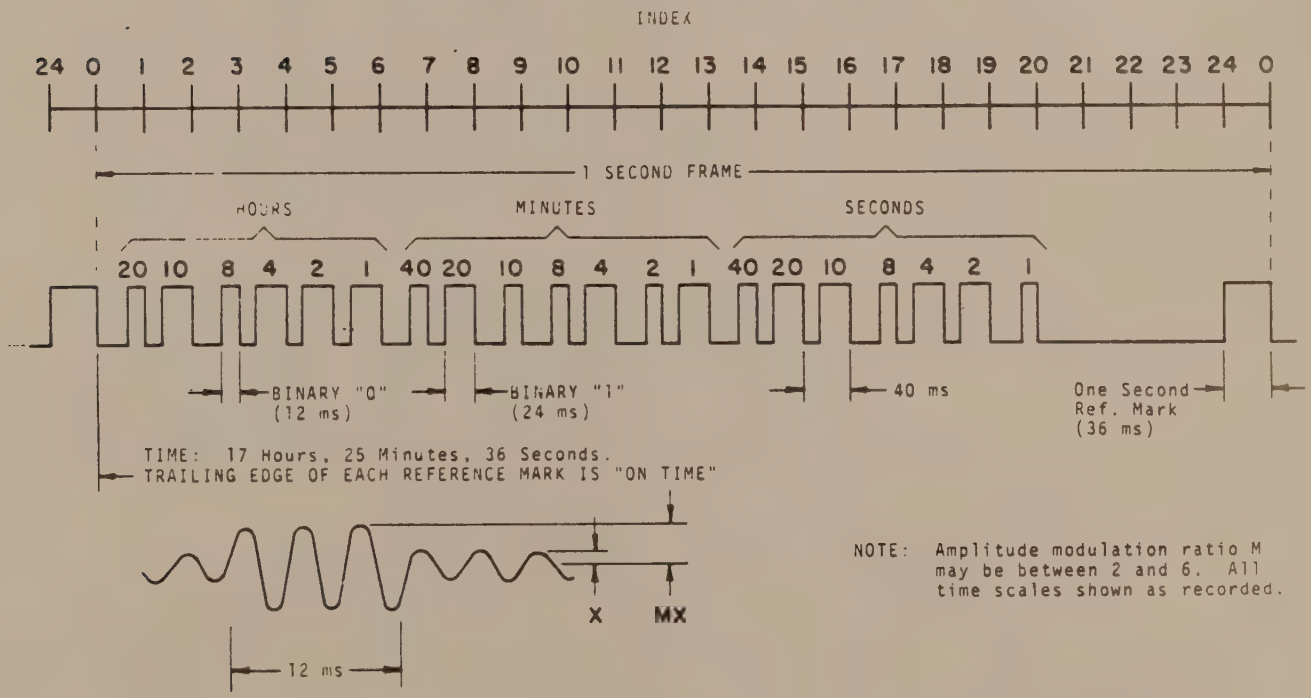
FIGURE 1.4 AMR TIME CODE FORMATS



AMR SIGNAL DESIGNATIONS

AMR NO.	17-BIT, 24-HOUR BINARY CODE
B1, B2	1 PPS (pulse width); 1 PPS (modulated)
C1, C2	20 PPS (pulse width); 20 PPS (modulated)
D1, D5	100 PPS (pulse width); 100 PPS (modulated)

FIGURE 1.5 XR3 TIME CODE FORMAT


INDEX
24 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 0
1 SECOND FRAME
HOURS
MINUTES
SECONDS
20 10 8 4 2 1 40 20 10 8 4 2 1 40 20 10 8 4 2 1
BINARY "0" (12 ms)
BINARY "1" (24 ms)
40 ms
One Second Ref. Mark (36 ms)
TIME: 17 Hours, 25 Minutes, 36 Seconds.
TRAILING EDGE OF EACH REFERENCE MARK IS "ON TIME"
X
MX
12 ms

NOTE: Amplitude modulation ratio M may be between 2 and 6. All time scales shown as recorded.

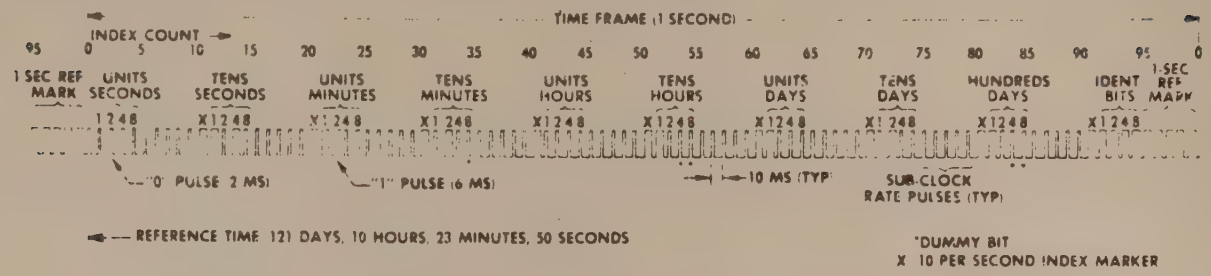
TYPICAL MODULATED CODE ELEMENT "ZERO" (250 Hz Carrier)

For 1 kHz carrier large amplitude cycles number 12, 24, and 36

FIGURE 1.6 NASA TIME CODE FORMATS

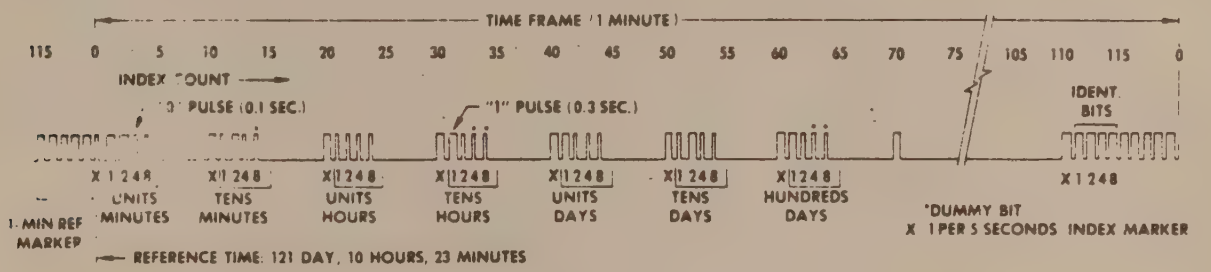
36-BIT, 100-PPS CODE (1000-CPS CARRIER)

SHOWING SUB-CLOCK RATE PULSES


TIME FRAME (1 SECOND)
INDEX COUNT
95 0 5 10 15 20 25 30 35 40 45 50 55 60 65 70 75 80 85 90 95 0
1 SEC REF MARK
UNITS SECONDS
TENS SECONDS
UNITS MINUTES
TENS MINUTES
UNITS HOURS
TENS HOURS
UNITS DAYS
TENS DAYS
HUNDREDS DAYS
IDENT BITS
1 SEC REF MARK
1 2 4 8
X 1 2 4 8
"0" PULSE 2 MS)
"1" PULSE (6 MS)
10 MS (TYP)
SUB-CLOCK RATE PULSES (TYP)
REFERENCE TIME 121 DAYS, 10 HOURS, 23 MINUTES, 50 SECONDS
*DUMMY BIT
X 10 PER SECOND INDEX MARKER

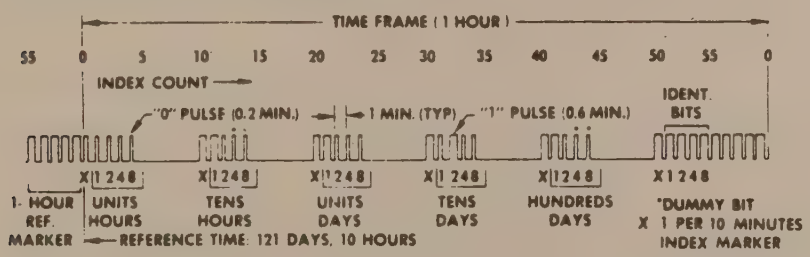
28-BIT, 2-PPS CODE (100-CPS CARRIER)

SUB CLOCK RATE PULSES INHIBITED

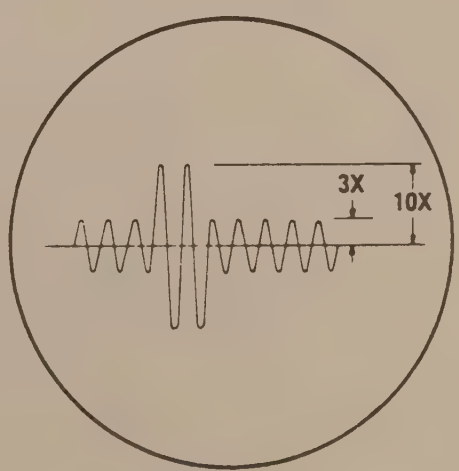

TIME FRAME (1 MINUTE)
115 0 5 10 15 20 25 30 35 40 45 50 55 60 65 70 75 105 110 115 0
INDEX COUNT
"0" PULSE (0.1 SEC.)
"1" PULSE (0.3 SEC.)
IDENT. BITS
X 1 2 4 8
UNITS MINUTES
TENS MINUTES
UNITS HOURS
TENS HOURS
UNITS DAYS
TENS DAYS
HUNDREDS DAYS
1-MIN REF MARKER
*DUMMY BIT
X 1 PER 5 SECONDS INDEX MARKER
REFERENCE TIME: 121 DAY, 10 HOURS, 23 MINUTES

20-BIT, 1-PPM CODE (100-CPS CARRIER)

SUB-CLOCK RATE PULSES INHIBITED



Insertion of sub-clock rate pulses is controlled for each format by individual control switches.



TYPICAL MODULATED SIGNAL

CHAPTER TWO
INSTALLATION

2.1 INITIAL INSPECTION

As soon as the instrument is received, verify that it is intact and as ordered. Inspect it for damage. If any shipping damage is found refer to the warranty at the front of this manual and to Section 2.2 for repackaging and shipping instructions.

As soon as possible, the instrument should be installed and given a thorough electrical inspection. Should the instrument fail to operate properly or fail to meet the listed specifications, immediately contact your Systron-Donner representative.

2.2 STORAGE AND RESHIPMENT

Environmental conditions during storage and shipment should be limited as follows:

Maximum Temperature: 185°F (85°C)

Minimum Temperature: -69°F (-55°C)

To protect your instrument during shipment or storage, use the best packaging methods available. Your Systron-Donner field office can provide materials similar to those used for original factory packaging. Contract packaging companies can provide dependable packaging on short notice.

General packaging instructions:

1) Wrap the instrument in heavy paper or plastic before placing it in the shipping container.

2) If possible, use the original container designed for the instrument. Otherwise, use a strong carton (350 lb. sq in. bursting strength) or wooden box to house the instrument.

3) Use plenty of packaging material around all sides of the instrument and protect the front panel with cardboard strips.

4) Seal the package with strong tape or metal bands. Mark the package with "DELICATE INSTRUMENT".

5) Refer to the warranty at the front of this manual and check with your Systron-Donner field office for shipping instructions. All correspondence should refer to the instrument by its model number and full serial number.

2.3 POWER AND COOLING REQUIREMENTS

The Model 8132, unless otherwise specified, is supplied to operate from a 115 V ± 10%, 48 to 62 Hz source.

To adapt the Model 8132 for 230 V operation, push the rear panel 115/230 V selector switch, S101, to the "230" position and change Fuse, F1, from 2 A slow-blow to 1 A slow-blow.

2.4 INITIAL ADJUSTMENT

To apply primary power to the Model 8132, it is only necessary to turn the READER MODE switch to PWR OFF, install the power cord (supplied), and turn the switch to READ 0E. Introduce the appropriate code via connector J8. The unit should translate and display the time information contained in the code, provided the input code is within specifications. No adjustment of the AGC (AGC/Cycle Detector card A10) should be necessary.

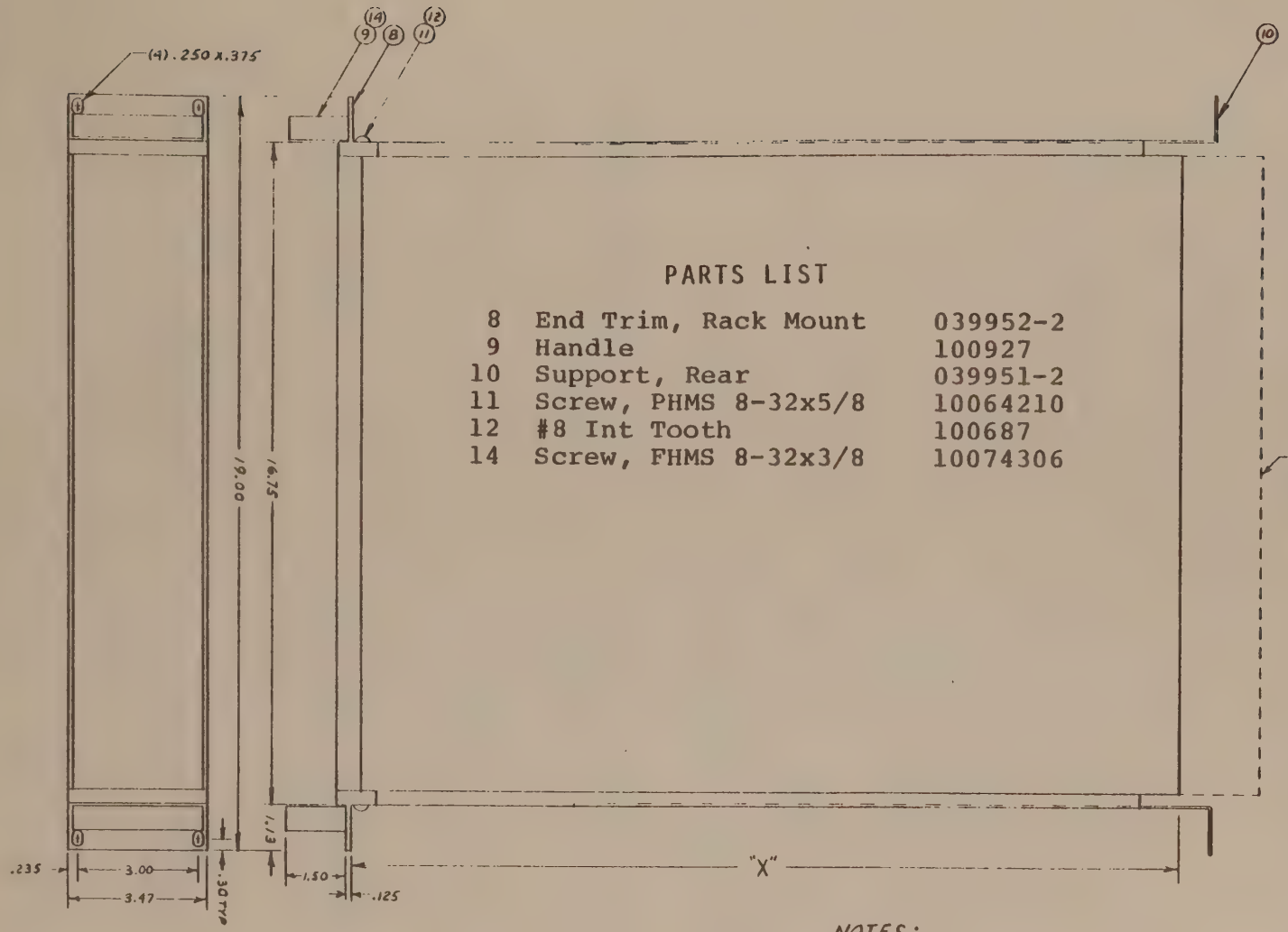
2.5 INSTALLATION

The Model 8132 is normally supplied with hardware for rack-mount installation as shown in Figure 2.1.

For convenience, the unit has been drilled for 20" Jonathan 120 QD series slides. When slides are used, the rear support brackets (Item 10) are removed.

NOTE

Under no condition should air flow through the outlet hole in the rear of the unit be obstructed.



PARTS LIST

8	End Trim, Rack Mount	039952-2
9	Handle	100927
10	Support, Rear	039951-2
11	Screw, PHMS 8-32x5/8	10064210
12	#8 Int Tooth	100687
14	Screw, FHMS 8-32x3/8	10074306

TABULATION

P/L #	"X"	INSTR. DEPTH
39986-1	8.75	9.12
39986-2	10.75	11.12
39986-3	12.75	13.12
39986-4	14.75	15.12
39986-5	16.75	17.12
39986-6	18.75	19.12
39986-7	20.75	21.12

NOTES:

1. INSTR. ARE DRILLED TO ACCEPT 20" JONATHAN 120 QD SERIES SLIDES
2. ITEM 10 DELETED WHEN SHIPPED W/SLIDES

FIGURE 2.1 3½" FULL RACK ASSEMBLY #039986-4-5 REV A

CHAPTER THREE
OPERATION

3.1 GENERAL

The Model 8132 is ready to operate immediately after turning on the power. Preliminary adjustments or calibration are not normally required. It is advisable that the following description on use of the instrument controls and indicators be read before operating the unit.

3.2 CONTROLS, INDICATORS AND CONNECTORS

3.2.1 Front Panel

1) MODE Selector: (Rotary Switch S30) — Controls main power and selects mode of operation.

   PWR OFF: — Removes power to the unit.

   READ OE: — Places the unit in a Read Mode condition which allows time information to be stripped from the input code and loaded into the display register.

   READ 3E: — Places the unit in a Read Mode condition such that transfer of time information into the display register is inhibited for up to three frames if an error is detected in forward.

2) TAPE DIRECTION: (Toggle Switch, S35) — NORMal position conditions unit to read a forward code. The REVerse position permits a reverse code to be read.

3) DISPLAY: — A 6-digit, in-line, planar readout which indicates TOD in hours, minutes and seconds. Days/ID option adds 3-digits.

4) TAPE ERROR: (LED, DSI) — Indicates a discrepancy between the input code and the contents of the display register when in Error Bypass Mode.

3.2.2 Rear Panel

1) BCD OUT/SEARCH CONTROL: (50-pin connector, J3) — BCD Output of display register contents plus search control signals.

2)	PULSE RATE: (14-pin connector, J4)	Pulse rate and control lines.
3)	CODE IN: (BNC connector, J8)	Modulated Code input to Reader.
4)	AC POWER: (AC connector, J101)	Mates with ac line cord.
5)	115/230 V Power Select: (Slide switch, S101)	Adapts power transformer for 115 or 230 volt operation.
6)	BCD MS, Optional: (14-pin connector, J6)	BCD milliseconds outputs.
7)	Remote, Optional: (36-pin connector, J7)	Reserved for options.
8)	SLOW CODE, Optional: (BNC connector, J11)	Slow time code output.
9)	365-366-ID, Optional: (Slide switch, S33)	Leap Year/ID selector switch (part of Days/ID option).
10)	Auxiliary, Optional: (50-pin connector, J5)	Reserved for options.

CHAPTER FOUR

MAINTENANCE AND CALIBRATION

4.1 FACTORY SERVICE

When the instrument requires service, the nearest Systron-Donner representative should be contacted. He can provide field service or arrange for factory returns, when necessary. Address all inquiries on operation or applications to your nearest sales representative; or Sales Manager:

SYSTRON-DONNER CORPORATION
CONCORD INSTRUMENT DIVISION
2727 Systron Drive
Concord, California 94518
Phone: (415) 676-5000
TWX: 910-481-9479
Cable: SYSTRON DONNER

Specify both model and complete serial number in all correspondence.

4.2 ROUTINE MAINTENANCE

A regular program for maintenance and inspection every five to six months is recommended for this unit. As part of these regular procedures, the instrument should be checked in the following manner:

1) Disconnect ac power and remove the top and bottom covers.

2) Make a thorough visual inspection of all wiring and cables. Check for frayed, loose, or burned wires.

3) Check the physical integrity of all components. Look for burned or cracked components, loose solder connections, leakage of insulation compounds, and general physical damage. When a printed-circuit board contains integrated-circuit packages, ensure that all packages are firmly mounted. Never unnecessarily remove and replace a package.

4) Check all front panel switches and controls for loose or broken terminals, loose or sticking shafts, etc.

5) If the internal panel surfaces and components have an excessive amount of dust deposited on them, use a soft brush and low-pressure stream of air to remove the foreign material.

CAUTION

Do not clean P.C. boards or small internal components with a stiff brush or solvents, since damage to the circuits may result. A high-powered vacuum cleaner device should not be used on small internal components.

6) Wipe the external surfaces of the instrument with a soft, damp cloth to remove dirt, fingerprints, and other foreign materials.

7) Replace the top and bottom covers and reconnect ac power. Perform the Operational Test and Calibration Procedure (Section 4.4). If performance does not match or exceed the specifications listed in Chapter 1 of this manual, corrective maintenance is in order.

4.3 PRINTED-CIRCUIT BOARD REPAIR

When replacing integrated circuits or other electronic components soldered to printed-circuit boards, the procedures indicated below must be followed or damage to the board may result:

1) Determine by troubleshooting techniques, which integrated circuit or discrete component(s) has failed.

2) Remove the defective component(s) from the board by cutting the pins or leads with a small diagonal clipping tool. (Always remove and replace the entire component).

3) Apply heat (40-50-W soldering iron) sparingly to each of the cut pins or leads and remove from the board; clean the hole(s) with a toothpick or solder suction tool.

4) Form the tinned leads of the replacement part and insert in the printed-circuit holes; solder, then trim leads to extend 1/16 inch beyond the back surface of the board. (Use only 63-37 solder with maximum 1/16 inch diameter).

CAUTION

Always trim semiconductor leads only after soldered installation is complete. This procedure greatly lessens the possibility of component failure due to shock-wave damage caused by the trimming tool.

5) When soldering semiconductor devices and all small components, be sure to use a heat sink tool or long-nosed plier connected to the component lead(s) while each is being soldered. Allow the solder connection to cool before removing the heat sink.

6) Clean all dirt and solder-flux from the printed circuit traces by liberal application of isopropyl alcohol or freon-type solvents.

4.4 OPERATIONAL TEST AND CALIBRATION PROCEDURE

In the event of an equipment malfunction the following circuit description and adjustment procedure, if followed in the listed sequence, will allow the service engineer to isolate the trouble to a particular circuit card or subsection.

When the trouble is isolated, the functional description in Chapter 5 and option information in Chapter 6 will facilitate repair.

WARNING

Dangerous high voltages are present in the power supply of this equipment. Use caution at all times when the protective covers are removed.

4.4.1 Recommended Test Equipment

The following test equipment or equivalent is recommended for use in servicing the Model 8132.

TABLE 4.1 TEST EQUIPMENT FOR MODEL 8132

Model	Manufacturer	Minimum Specifications
422	Tektronix, Inc.	Oscilloscope, 15 MHz bandwidth, triggered sweeps from 0.1 microseconds/cm to 5 sec/cm. Vertical sensitivity from .05 volts/cm to 20 volts/ cm.
6012	Tektronix, Inc.	Probe, 10:1 attenuation ratio, 17 pF capacitance.
7003	Systron-Donner Corp.	DMM 10 MΩ input impedance, ±0.1% accuracy.
200AB	Hewlett Packard	Audio Oscillator, 20 Hz to 40 kHz coverage.
6250	Systron-Donner Corp.	Frequency Counter, 0 Hz to 50 MHz, 3 parts/10^7 per week.

In addition to the equipment listed above, a suitable source of time code input signals with known characteristics is required. This may be a Time Code Generator or a prerecorded tape and tape playback equipment.

4.4.2 Power Supply (Dwg. #41810-7-9)

The voltage checks listed below will ensure the correct operation of the power supply, assuming a normal line voltage of 115 V ac.

The voltages listed below are unregulated and nonadjustable. The test points are available on the unit PC edge connector, P103.

1) Ensure the presence of +210 V dc ±25% at pins V,18 (fuse F2).

2) Ensure the presence of +21 V dc ±20% at pins S,15 (fuse F3).

3) Ensure the presence of +9 V dc ±20% at pins Y,21.

4) Ensure the presence of -9 V dc ±20% at pin 2.

5) Ensure the presence of -21 V dc ±20% at pin 4.

4.4.3 Power Supply Regulator (Dwg. #41810-7-9)

Adjust the following voltages on the Power Supply Regulator board. The test points are located on the power supply PC board (Dwg. #41804-4-9) near the adjustment potentiometers.

TABLE 4.2

POWER SUPPLY REGULATOR VOLTAGE ADJUSTMENTS

Voltage	Adjust	Test Point
+15 V dc ±0.5%	R5	Blue
-15 V dc ±0.5%	R5	Violet
+5 V dc ±0.5%	R19	Red
-5 V dc ±0.5%	R19	Green

If the Power Supply Regulator is operating normally, and the unregulated voltages are correct, the above voltages will be obtained with little difficulty. If they do not adjust properly, or fail to maintain regulation, corrective maintenance is in order.

4.4.4 AGC & Cycle Detector (Dwg #21569-7-1)

1) Preliminary Set-Up

   a) Connect a time code source to "CODE IN" BNC connector on rear panel of the unit (signal level approximately 3 volts peak-to-peak).

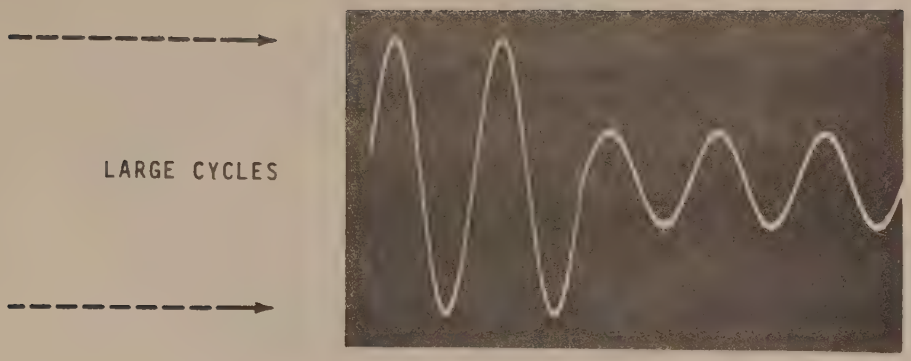


FIGURE 4.1 AGC LEVEL ADJUSTMENT

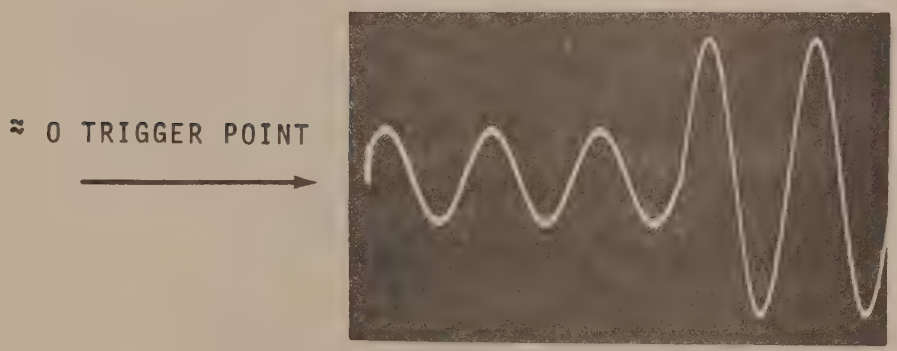


FIGURE 4.2 CYCLE DETECTOR ADJUSTMENT

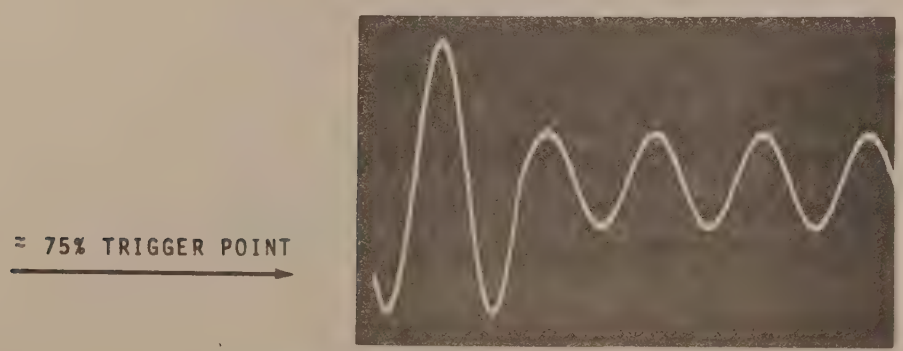


FIGURE 4.3 LOWER LARGE CYCLE ADJUSTMENT

b) Place unit in either Read Mode.

CAUTION

Do not place AGC & Cycle Detector on extender board when performing these adjustments.

2) AGC Level

a) Monitor "TRIG" test point with oscilloscope.

(1) Adjust "AGC" potentiometer R4 so that the large cycles (see Figure 4.1 AGC Level Adjustment) are 2.75 volts peak-to-peak ±5%.

(2) Reduce level of incoming time code signal to approximately 1 volt peak-to-peak.

Allow approximately 5 seconds for AGC to recover. Signal at "TRIG" test point should remain the same amplitude as adjusted in Step (1).

3) Cycle Detector

a) Monitor "TRIG" test point with oscilloscope

(1) EC, Each Cycle,Adjustment.

Set oscilloscope to trigger positive (+), external trigger. Connect external trigger input of oscilloscope to "EC" test point.

Turn R25 "EC" Adjust, full clockwise. Turn in the CCW direction until each cycle is triggering approximately 30% up on the positive slope of the small cycles (see Figure 4.2, Cycle Detector Adjustment).

(2) LLC, Lower Large Cycles Adjustment

Set oscilloscope to trigger negative (-), external trigger. Connect external trigger input of oscilloscope to $\overline{\text{LLC}}$ test point.

Turn R34 "LLC" Adjust, full clockwise. Turn in the CCW direction until the lower large cycles are triggering approximately 75% of the way down on the negative slope of the lower large cycles (see Figure 4.3 Lower Large Cycle Adjustment).

4.4.5 Reverse Operation

With the Model 8132 in either Read Mode, check that it will read in the forward and reverse directions as follows: Place the TAPE DIRECTION

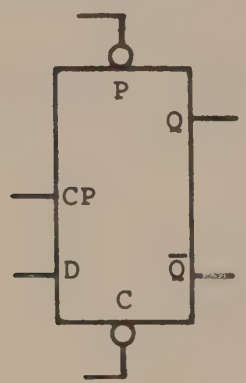
EXCLUSIVE OR

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

EXCLUSIVE NOR

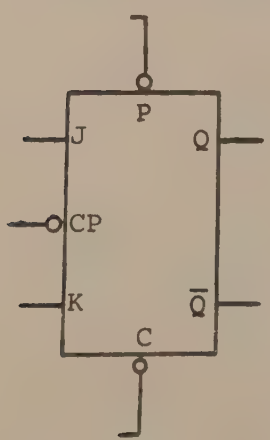
A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

D-TYPE Flip-Flop



1) Q assumes the state of the D input on the positive transition of the clock (CP) input.
2) The D input is locked out when the clock input is positive.
3) P and C override all other inputs.
4) If $\overline{P}$ and $\overline{C}$ are both at Logic 0, the Q and $\overline{Q}$ outputs are both at Logic 1.
5) At a set condition, Q is Logic 1. At a clear condition, Q is a Logic 0.

JK-TYPE Flip-Flop



1) When J and K are both at a Logic 0, no change will occur.
2) When K is a Logic 1, Q will be a Logic 0.
3) When J is a Logic 1, Q will be a Logic 1.
4) When J and K are both at a Logic 1, the flip-flop will change state.
5) $\overline{P}$ and $\overline{C}$ override all other inputs.
6) CP is the clock input.

CHAPTER FIVE
FUNCTIONAL DESCRIPTION

5.1 GENERAL

The Model 8132 is a Time Code Reader capable of translating a modulated time code in either the forward or reverse direction. Schematics and specific card assembly descriptions relating to the basic unit are provided at the end of the chapter. Standard options, when included, are described in Chapter 6. Special modifications, if any, are presented in Chapter 7.

5.1.1 Reference Designations

Reference designations are confined to the assembly under discussion since it is usually clear from the contest which assembly is involved.

When citing a subelement of a multielement integrated circuit, the reference designation of the integrated circuit is given, followed by the number of the output terminal.

When citing flip-flops formed from two gates on the same chip, the reference designation of the chip is given followed by the two output pin numbers. The reference designations used in the Model 8132 are listed in Table 5.1.

TABLE 5.1
REFERENCE DESIGNATIONS

A or U	Integrated Circuit
C	Capacitor
CR	Diode
DS	Lamp
F	Fuse
FL or Z	Filter
J	Jack
L	Inductor
P	Plug
Q	Transistor
R	Resistor
S	Switch
T	Transformer
TP	Test Point
W	Jumper
X	Socket

5.1.2 Logic Functions

The Logic symbols and functions used in the Model 8132 are described as follows:

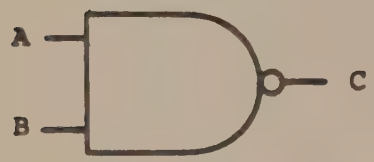
AND Gate

INVERTED NOR Gate

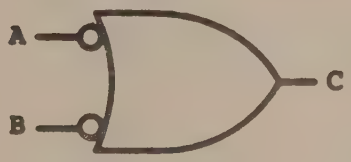
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

The AND Gate and INVERTED NOR Gate have the same truth table.

NAND Gate



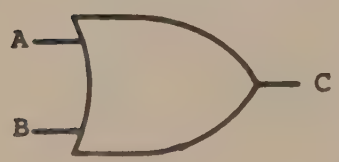
INVERTED OR Gate



A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

The NAND Gate and INVERTED OR Gate have the same truth table.

OR Gate



INVERTED NAND Gate

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

The OR Gate and INVERTED NAND Gate have the same truth table.

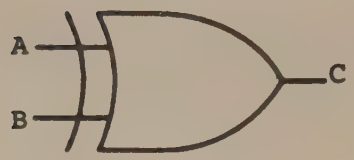
NOR Gate

INVERTED AND Gate

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

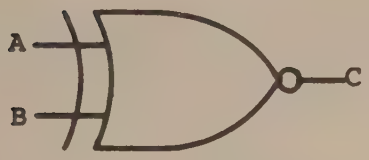
The NOR Gate and INVERTED AND Gate have the same truth table.

EXCLUSIVE OR



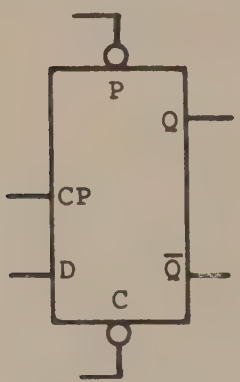
A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

EXCLUSIVE NOR



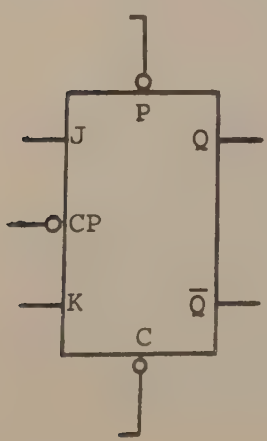
A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

D-TYPE Flip-Flop



1) Q assumes the state of the D input on the positive transition of the clock (CP) input.
2) The D input is locked out when the clock input is positive.
3) P and C override all other inputs.
4) If $\overline{P}$ and $\overline{C}$ are both at Logic 0, the Q and $\overline{Q}$ outputs are both at Logic 1.
5) At a set condition, Q is Logic 1. At a clear condition, Q is a Logic 0.

JK-TYPE Flip-Flop



1) When J and K are both at a Logic 0, no change will occur.
2) When K is a Logic 1, Q will be a Logic 0.
3) When J is a Logic 1, Q will be a Logic 1.
4) When J and K are both at a Logic 1, the flip-flop will change state.
5) $\overline{P}$ and $\overline{C}$ override all other inputs.
6) CP is the clock input.

In some configurations it is possible to perform the AND and OR functions simply by tying the outputs of certain gates together.

These functions are called DOT AND and DOT OR functions. The nature of the signals fed to the "DOT" determines whether the function is AND or OR. When several "DOTS" are present on a single line the AND or OR symbol is used only once.

DOT AND

DOT OR

5.2 Function

The Model 8132 Time Code Reader accepts a serial modulated IRIG B time code input. It strips time informations from the code in bytes and loads it into the TOD Accumulator. The time in the accumulator is displayed. It is also available for output in parallel through buffers on card A16. Circuits are included to maintain the accumulator on time in forward mode and to regenerate a serial code for comparison with the input in the Error Bypass mode of operation. (Days/ID and/or the translation of other time codes may be included as options). The basic Reader is shown in block form on Drawing #06103402.

5.2.1 AGC/Cycle Detector (Dwg. #021569-7-1)

Referring to the block diagram, the modulated input code is fed through connector J8 to AGC/Cycle Detector card (A10). The AGC circuit on this card establishes a standard level signal from which two signals are derived. The first of these is the EC (Each Cycle) signal which is a square wave at the carrier frequency. The second is the $\overline{\text{LLC}}$ (Lower Large Cycle) signal. Both signals are fed to Reader Logic card (A12). The EC signal is also fed through selection gates on Preset and Error Bypass card (A11), emerging as the $\overline{\text{Z-RATE}}$ signal to the Minor Couter card (A9) and Code Generator card (A17).

5.2.2 Reader Logic (Dwg. #021588-7-3)

The Reader Logic card (A12) contains a 9-bit shift register which accumulates time information stripped from the input code. This register is cleared and a ONE entered by the double-mark at the beginning of the time frame. This is followed by each subsequent bit as it is detected. When the initial ONE is in the 9 position, the contents of the shift register are transferred into the seconds section of the TOD Accumulator card (A15). The next index mark clears the register and enters a ONE followed by minutes information. These bits are transferred to the minutes section of the accumulator. In like manner, hours (and days) bits are detected and transferred. (Days are loaded into Days Accumulator A18 when the Days/ID Option is included.)

5.2.3 Minor Counter (Dwg. #021632-7-2)

Once the Time Code Reader is synchronized with the input code (in forward), the TOD Accumulator card (A15) plus A18 with Option E13, already contains the current information being transferred in. This is accomplished by the Minor Counter card (A9) which derives a 1 pps, on-time update pulse from the Z-RATE signal. This signal updates the accumulator on-time at the beginning of each frame.

The Minor Counter card (A9) is a three-decade divider which divides the 1 KHz (Z-RATE) input down to 1 pps to drive the TOD Accumulator (card A15) and provide a sync signal for Code Generator card (A17). A separate set of buffers are provided for parallel BCD milliseconds outputs for Option E14 (Millisecond Outputs). Pulse rates (1 Kpps, 100 pps, 10 pps and 1 pps) are provided at connector J4.

5.2.4 TOD Accumulator (Dwg. #021543-7-3)

The TOD Accumulator card (A15) accepts the 1 pps (8×10^{-1}) output from the Minor Counter card (A9) and divides it into units and tens-of-seconds, minutes and hours. The decade and scale-of-six dividers which accomplish this can be parallel preset, as well as provide parallel BCD outputs. This permits the time stripped from the input code by the Reader Logic card (A12) to be loaded. The parallel BCD outputs feed: 1. The Display Assembly (A102); 2. the Code Generator (A17); and, 3. Buffer (A16) to provide TOD outputs. The 1 ppd output is fed to Days Accumulator (A18) as parts of Option E13, Days/ID. See Chapter Six.

5.2.5 Code Generator (Dwg. #021554-7-1)

The Code Generator card (A17) accepts the parallel TOD inputs and developes a serial level shift code complete with index and frame markers. Days/ID are replaced by zeros in the code in the absence of Option E13. The level shift code is fed to Preset and Error Bypass card (A11).

5.2.6 Preset and Error Bypass (Dwg. #7-05153802)

The serial level shift code from the Code Generator card (A17), containing the time from the accumulator, is compared with the incoming code in circuits on Preset and Error Bypass card (A11). When operating in the Error Bypass mode, this circuitry inhibits the transfer of up to three consecutive input code frames if a discrepancy is detected.

5.2.7 FWD-REV Control

The Time Code Reader is capable of reading the input code in the reverse direction as well as forward except that Error Bypass does not function in reverse. The conditions for reverse read operation are established by circuits on FWD-REV Control card (A13) in response to signals from the TAPE DIRECTION switch or the REV input through connector J3. Circuits on card (A13) invert the order in which bits are transferred to the Accumulator, suppress the 1 pps update signal and inhibit Error Bypass when reading a reverse code. In reverse, the contents of the Accumulator are no longer on-time.

5.4 CIRCUIT DESCRIPTIONS

The Circuit Descriptions contained in this Chapter are used in several Systron Donner Models. As a result, references may be made to control lines, circuits or functions which are not applicable to the Model 8132. Notables references to PRESET and GENerate circuits (although contained, in part, on some of the PC boards), are inoperative and these sections should be disregarded.

TABLE 5.2

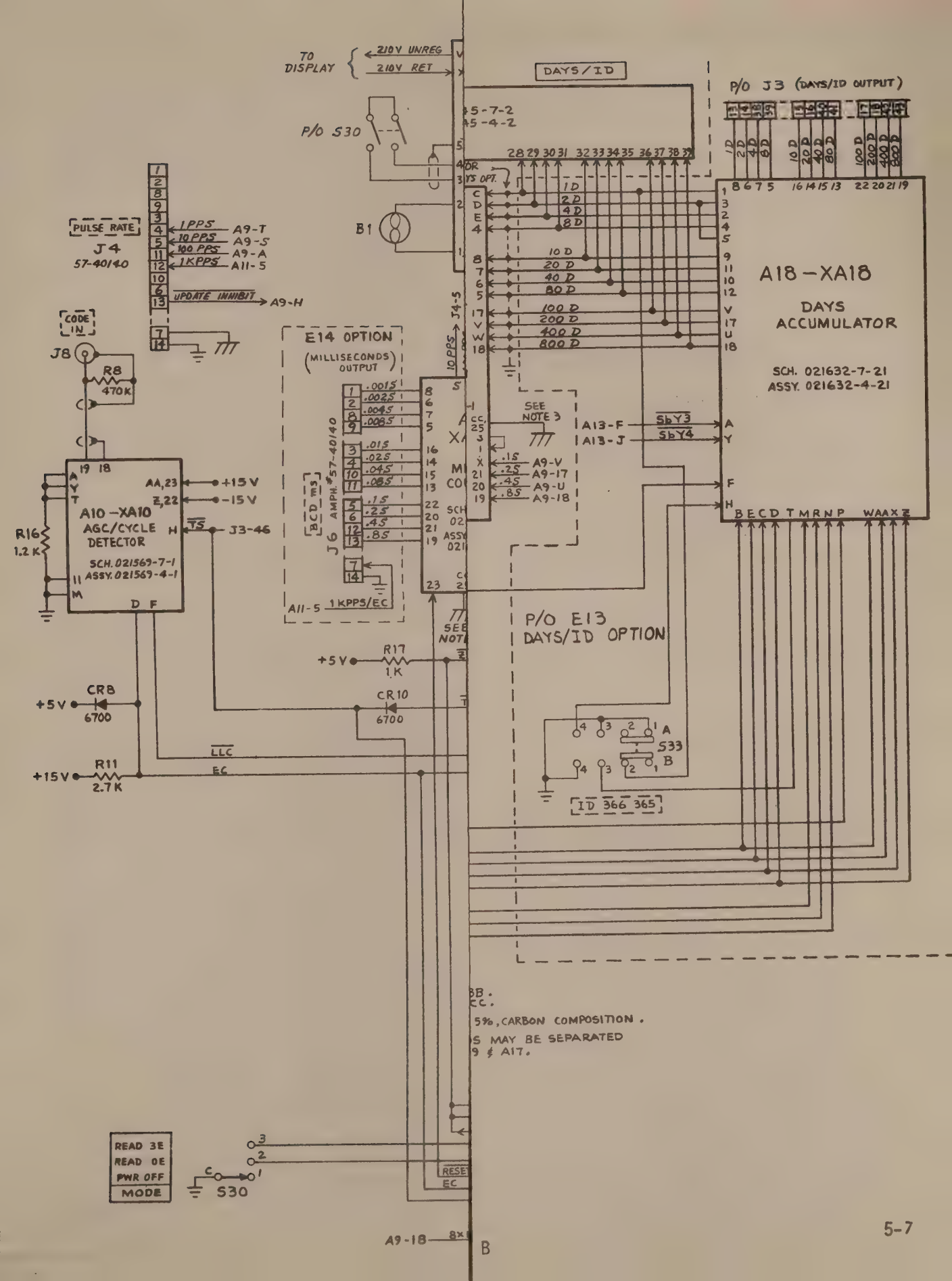
CIRCUIT DESCRIPTION INDEX INFORMATION

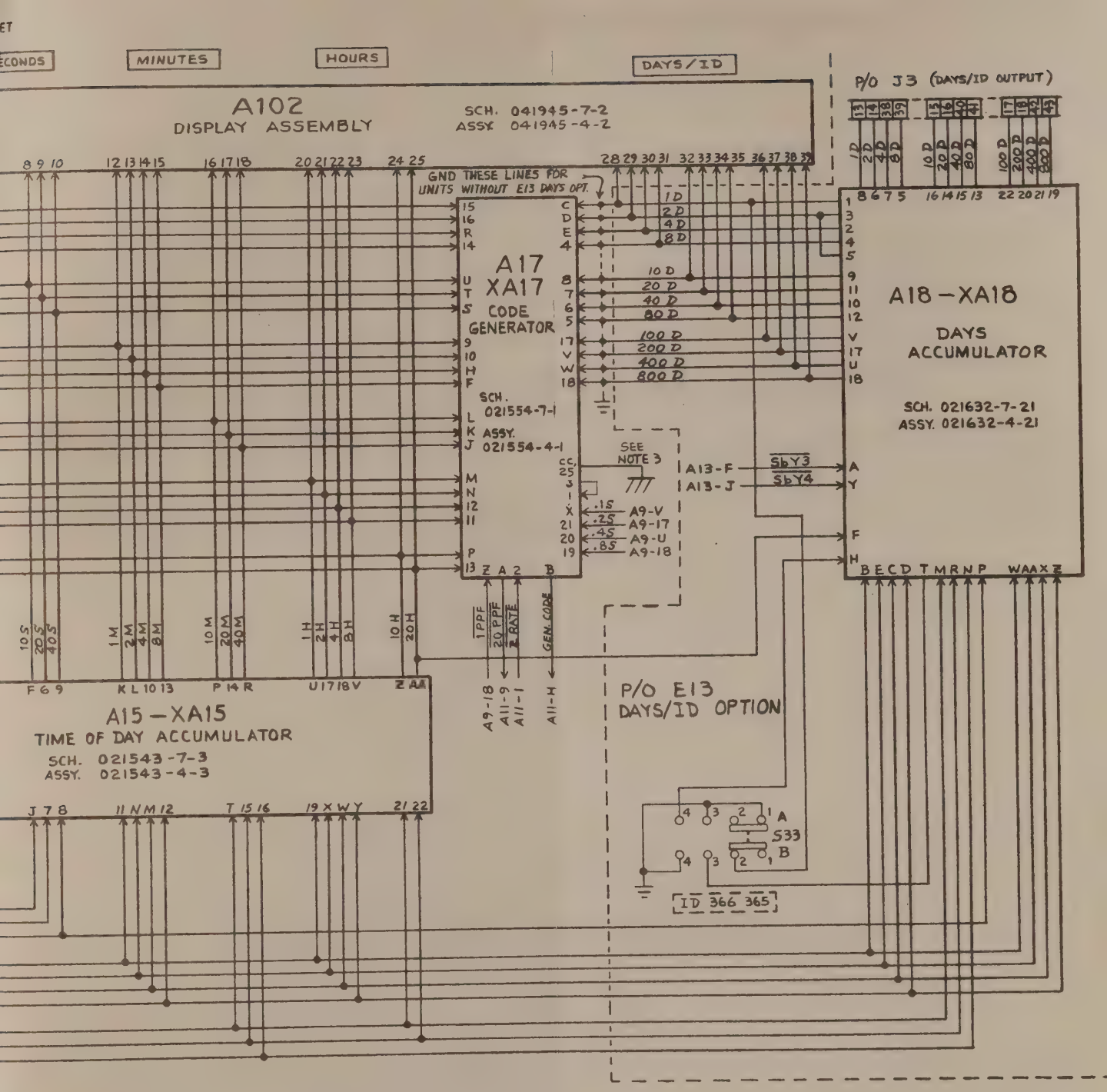
LOCATION	DESCRIPTION	SCHEMATIC #	PAGE #
A1-A8	Reserved for Options		
A9	Minor Counter	021632-7-2	5-39
A10	AGC/Cycle Detector	021569-7-1	5-25
A11	Preset and Error Bypass	05153802	5-44
A12	Reader Logic	021588-7-3	5-30
A13	FWD-REV Control	021625-7-1	5-35
A14	Reserved for Options		
A15	TOD Accumulator	021543-7-3	5-14
A16	Buffer	021535-7-3	5-10
A17	Code Generator	021554-7-1	5-18
A18	Days Accumulator (Optional)	021632-7-21	6-E13-3
A19-A27	Reserved for Options		
A101	Power Supply	041810-7-9	5-49
A102	Display Assembly	041945-7-2	5-58

All plug-in modules are designed so that the card will only fit into position if it is correctly aligned; however, caution must be exercised to ensure that a card is installed in the correct card slot. Extractor handles on all cards are numbered to facilitate correct installation.

CAUTION

When mounting a card on the extender board, it is possible to install the card backwards which will result in serious damage.


TO DISPLAY
210V UNREG
210V RET
P/O S30
DAYS/ID
P/O J3 (DAYS/ID OUTPUT)
5-7-2
5-4-2
B1
PULSE RATE
J4
57-40140
1 PPS
10 PPS
100 PPS
1 KPPS
A9-T
A9-S
A9-A
A11-5
UPDATE INHIBIT
A9-H
CODE IN
J8
R8
470K
E14 OPTION
(MILLISECONDS OUTPUT)
J6 AMPH. #57-40140
BCD
.0015
.0025
.0045
.0085
.015
.025
.045
.085
.15
.25
.45
.85
A11-5 1 KPPS/EC
10 PPS
J4-5
1D
2D
4D
8D
10D
20D
40D
80D
100D
200D
400D
800D
A18-XA18
DAYS ACCUMULATOR
SCH. 021632-7-21
ASSY. 021632-4-21
SEE NOTE 3
A13-F
A13-J
SbY3
SbY4
A9-V
A9-17
A9-U
A9-18
A10-XA10
AGC/CYCLE DETECTOR
SCH. 021569-7-1
ASSY. 021569-4-1
+15V
-15V
J3-46
R16
1.2K
R17
1K
+5V
CR8
6700
CR10
6700
R11
2.7K
LLC
EC
P/O E13
DAYS/ID OPTION
S33
ID 366 365
READ 3E
READ 0E
PWR OFF
MODE
S30
RESET
EC
A9-18
8X
B
5%, CARBON COMPOSITION.
S MAY BE SEPARATED
9 & A17.



NOTES

1) +5V IS ON P.C. CARD PINS 24 & BB.
   GND IS ON P.C. CARD PINS 25 & CC.
2) RESISTORS ARE IN OHMS, ¼W, 5%, CARBON COMPOSITION.
3) CHASSIS AND SIGNAL GROUNDS MAY BE SEPARATED BY REMOVING GND LUGS AT A9 & A17.

TIME CODE READER BLOCK DIAGRAM #06103402 REV B

PARTS LIST

FINAL ASSEMBLY #06103402

REFERENCE	DESCRIPTION	SD PART NO.
	SHIPPING ASSEMBLY REV B	#06103402
	Assembly, Test	06115502
	Trim, Front Panel	041997-1-1
	Trim, Side	039859-5
	Trim, End Rack Mount	03995202
	Window	051001-1-1
	Cover, Mounting Bracket	039857
	Cover, Top	03376005
	Cover, Bottom	03376105
	Support, Rear	03995102
	Handle	100927
P3	Connector, 50 Pin	101157
P4	Connector, 14 Pin	101181
P101	Line Cord	102407
	Foil Cal	037112
	TEST ASSEMBLY REV B	#06115502
	Assembly, Front Panel	06115301
	Assembly, Rear Panel	06115401
A101	Assembly, Power Supply	041810-4-9
A9	Assembly, Minor Counter	021632-4-2
A10	Assembly, AGC/Cycle Detector	021569-4-1
A11	Assembly, Preset/Error Bypass	05153802
A12	Assembly, Reader Logic	021588-4-3
A13	Assembly, FWD-REV Control	021625-4-1
A15	Assembly, TOD Accumulator	021543-4-3
A16	Assembly, Buffer	021535-4-3
A17	Assembly, Code Generator	021554-4-1
A29	Assembly, Extender	021507-4-1
C1	Capacitor, 100 pF	100173
CR8,10,12	Diode, 6700	006700
R8	Resistor, 470K ¼w 5%	101630
R11	Resistor, 2.7K ¼w 5%	101599
R16	Resistor, 1.2K ¼w 5%	101581
R17	Resistor, 1K ¼w 5%	101569
	Card Rack, Front	08115501
	Card Rack, Rear	08115502
	Gusset, Left	041809-1-1
	Gusset, Right	041809-1-2
	Card Guide	021340-1-2
	Schematic	7-06103402

PARTS LIST

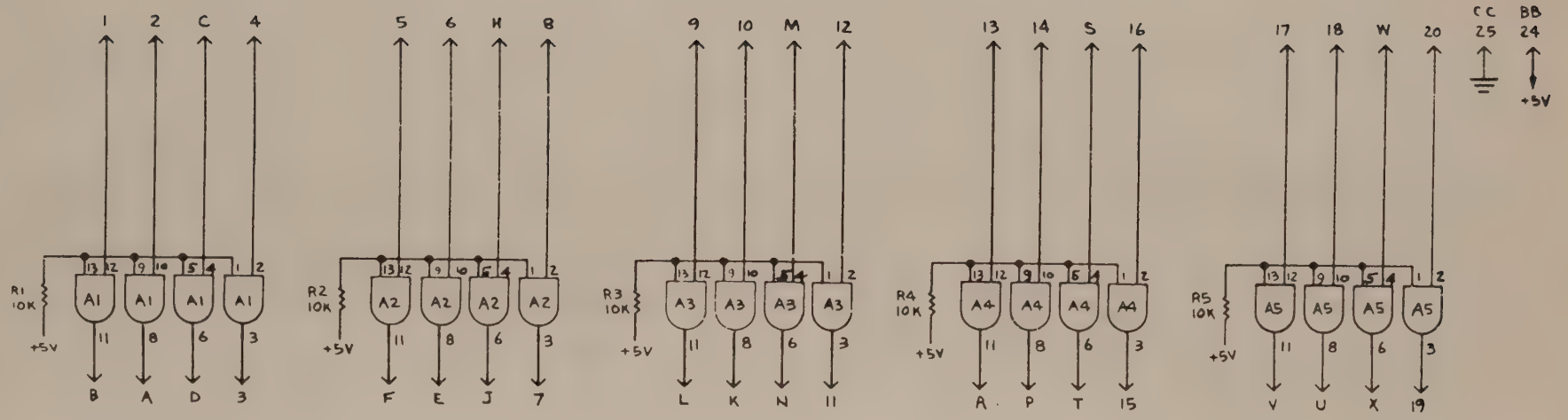
FINAL ASSEMBLY #06103402 (CON'T)

REFERENCE	DESCRIPTION	SD PART NO.
	TEST ASSEMBLY (CON'T)	#06115502
XA9-13,15-17,39	Connector, PC Edge	101204
XA101	Connector, Modification	051066-4-1
	Key	102653
P102	Shell	101263
	Standoff	100494
	Terminal, Male	10282202
	Spacer, Power Supply	051121-1-1
	FRONT PANEL ASSEMBLY REV C1	#06115301
	Sub Front Panel	061171
	Nomen Panel	061150
	Trim Strip	041773-1-1
DS1	Lamp, LED	100456
	Dress Nut	100893
	Display Assembly	041945-4-2
S30	Switch, Rotary	06134401
S35	Switch, Toggle SPDT	102310
	Knob	102954
	REAR PANEL ASSEMBLY REV D	#06115401
	Rear Panel	041815-1-2
B1	Fan	100038
	Fan Screen	100886
	Cover Plate, Oscillator	051913
	Cover Plate, 14 Pin	021398-1-1
	Cover Plate, 36 Pin	031124-1-1
	Cover Plate, 50 Pin	031394-1-1
	Hole Plug, BNC	100952
J3	Connector, 50 Pin	101136
J4	Connector, 14 Pin	101180
J8	Connector, BNC	101155
	Insulator, BNC	100823
	Washer, Fiber	101074
S1,15	Switch, Cover Plate	05120801
S16	Switch, Cover Plate	05120802
	#6 Flat Washer	100704

CIRCUIT DESCRIPTION
BUFFER ASSEMBLY
SCHEMATIC #021535-7-3 REV A_1

1) GENERAL

This card contains 20 integrated-circuit gates, connected as non-inverting buffers. It is used to buffer the seconds through hours outputs of the Time-of-Day Accumulators. A binary "1" output is 5 V (±0.5V) 6 K source. A binary "0" outputs is 0 V (±0.5V) 12 mA sink.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE IN OHMS, 1/4W, 5%.
2. PIN 14 OF ALL I.C.'S IS CONNECTED TO +5V & PIN 7 " " " " " " GRD.
3. A1 THRU A5 ARE MC1806P

BUFFER SCHEMATIC #021535-7-3 REV A_1

PARTS LIST

BUFFER #021535-7-3 REV A_1

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly	021535-4-3
	Schematic	021535-7-3
A1-5	Integrated Ckt, MC1806P	025733
R1-5	Resistor, 10K ¼w 5%	101570
	Extractor	100865
	Roll Pin	100752

CIRCUIT DESCRIPTION

TIME-OF-DAY ACCUMULATOR

SCHEMATIC #021543-7-3

1) GENERAL

This card successively divides the 1 pps signal to provide outputs which represent seconds through hours. All outputs are buffered, an input inhibit circuit is provided, and the dividers are recycled to zero one second after reaching 23:59:59.

2) DIVIDERS

Dividers U1, U4, U7 and U8 are divide-by-10 circuits. Dividers U3 and U5 are divide-by-8 circuits. Recycle circuits formed from gates on U13 and U17 convert U1, U3 to a scale of 60, U7, U8 to a scale of 60 and U7, U8 to a scale of 24. Each divider has its data inputs, connected to a preset time source. Grounding the appropriate preset line will load the preset time into divider. Grounding pin 23 resets the Accumulator through gates on U9, U13 and U17.

3) RECYCLE CIRCUITS

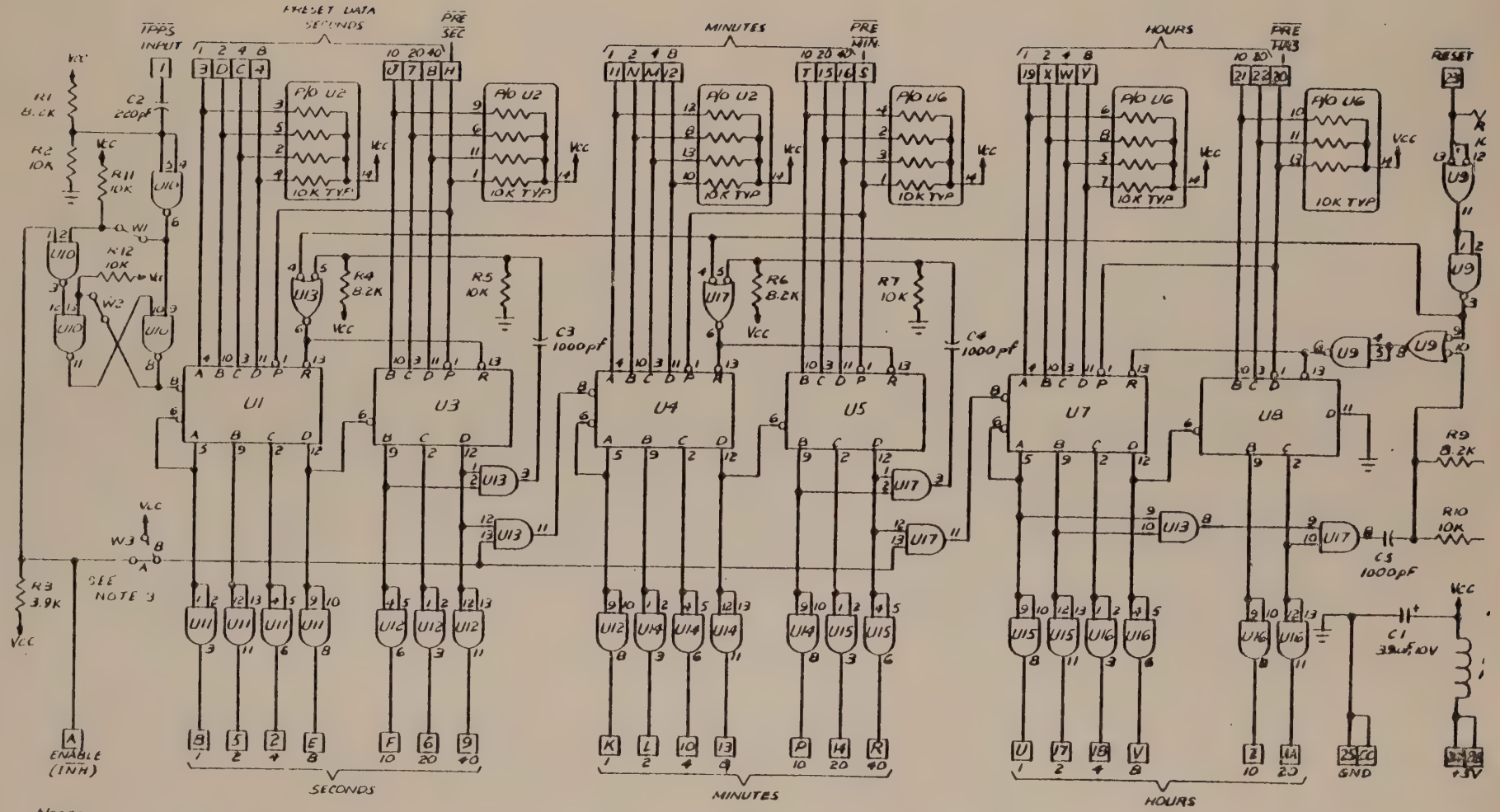
The scale of 60 recycle circuits for seconds and minutes are identical. The seconds circuit consists of AND gate U13-9 and a differentiating circuit formed from C3, R4 and R5. Gate U13-9 output goes high when U3 reaches a count of 5. It resets U1 and U3 through C3 and U13-6 when it returns low at the next count.

The scale of 24 recycle circuit for hours consists of AND gates U13-8, U17-8 and a differentiating circuit formed from C5, R9 and R10. The output from U17-8 goes high when U7 and U8 reach a count of 23. It resets U7 and U8 through C5 and U9-8,6 in tandem when it returns low at the next count.

4) INHIBIT CIRCUIT

The inhibit circuit is used to stop updating of the accumulator when the unit is in HOLD. Gate U10-6 inverts the 1pps input. Gates U10-8,11 form an RS flip-flop. Gate U10-3 inverts the $\overline{\text{INHIBIT}}$/ENABLE line, pin A. When this line is grounded, the flip-flop will latch with the output high. The output will go low the first time the input is low after the ground has been removed from the $\overline{\text{INHIBIT}}$/ENABLE input.

Programming jumper W3 is installed in the "A" position in Readers and Reader/Generators to prevent update of minutes and hours in reverse read operation. It is installed in the "B" position in Clocks and Generators where the ENABLE input to Pin A is used for HOLD.



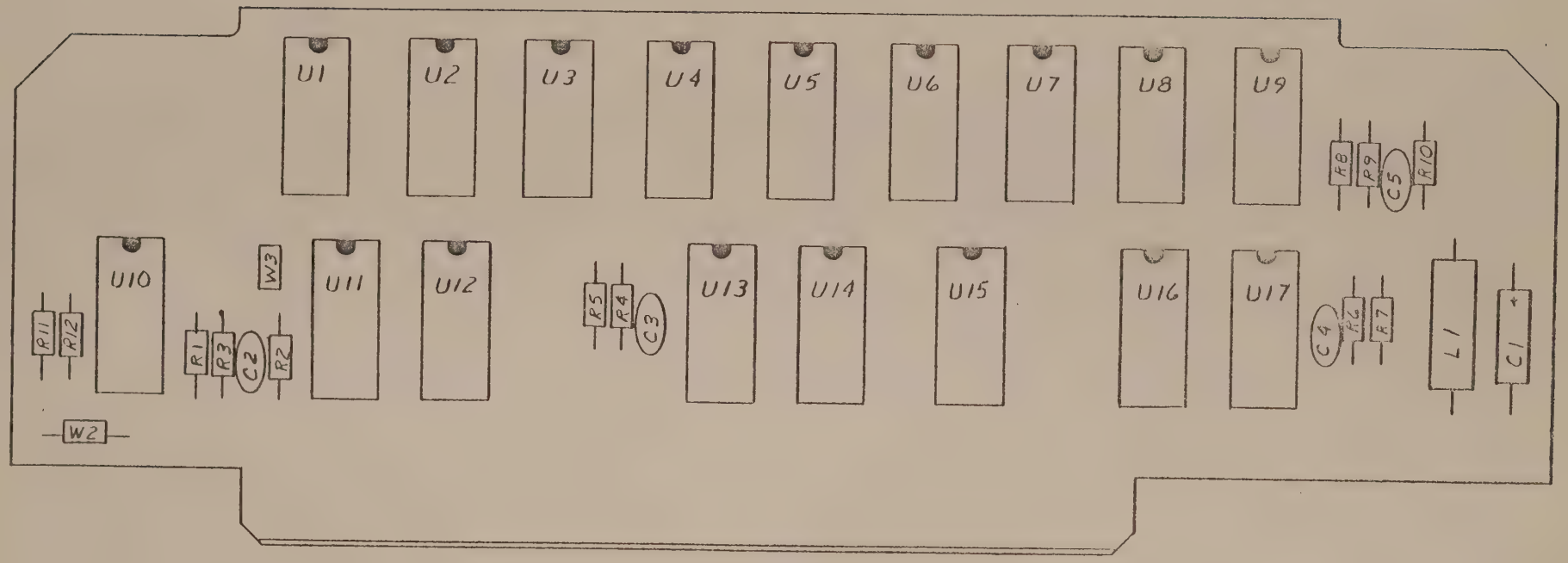
NOTES:

1. RESISTORS ARE ¼W, 5%, CARB. COMP.
2. I.C.'S

		VCC	GND
U1, U4, U7, U8	74LS196	14	7
U2, U6	RES PACK(10K)	14	-
U3, U5	74LS197	14	7
U9	74LS132	14	7
U10	846	14	7
U11, U12, U13, U14, U15, U16, U17	7408	14	7

3. PROGRAMMING JUMPER W3 IS INSTALLED IN THE "A" POSITION IN READER & READER/GENERATORS TO PREVENT UPDATE OF HOURS & MINUTES IN REVERSE READ. IT IS INSTALLED IN THE "B" POSITION IN CLOCKS & GENERATORS WHERE THE ENABLE INPUT TO PIN A IS USED FOR HOLD.

TOD ACCUMULATOR SCHEMATIC #021543-7-3 REV F



TOD ACCUMULATOR ASSEMBLY #021543-4-3 REV E

PARTS LIST
TIME-OF-DAY ACCUMULATOR #021543-7-3

REF.	DESCRIPTION	SD PART NO.
	Assembly	021543-4-3
	Schematic	021543-7-3
C1	Capacitor, 39 µF	100183
C2	Capacitor, 220 pF	117633
C3,4,5	Capacitor, 1000 pf	117639
R1,4,6,9	Resistor, 8.2K ¼w 5%	10159501
R2,5,7,8,10,11,12	Resistor, 10K ¼w 5%	10157001
R3	Resistor, 3.9K ¼w 5%	10160101
U1,4,7,8	Integrated Ckt, 74LS196	103164
U2,6	10K Resistor Pack	117241
U3,5	Integrated Ckt, 74LS197	103165
U9	Integrated Ckt, 74LS132	116946
U10	Integrated Ckt, 74LS00	103130
U11 - U17	Integrated Ckt, 7408	103093
L1	Inductor, R45-4	101313
W2	Molded Jumper	102879
W3	Shorting Jack Mod.	08126101
	Shorting Jack	116979
	Pin, Swage	116978
	Extractor	100865

CIRCUIT DESCRIPTION
CODE GENERATOR
SCHEMATIC #021554-7-1

1) GENERAL

The IRIG DC Code Generator card can be used to generate the IRIG A, B, C, E, or H codes. Code selection may be remotely controlled or fixed by the particular card configuration. Days information may be optionally included and provision is made for the insertion of control function bits and/or straight binary seconds from a source external to the card. The following description is intended to apply in general to all configurations of the card. The specific assembly used is identified by the attached assembly, schematic and parts list.

2) DIVIDER CIRCUITS

Refer to the timing diagrams and the schematic for this and subsequent sections. Divider A8 is a divide-by-two, then-by-five counter which divides down the "Z" RATE" and provides decoded outputs for the code generating gates. Divider A15 is a divide-by-five, then-by-two counter which takes the output of A8, divides it down and supplies decoded outputs for the scan gates and the code generating gates. Divider A17 is a divide-by-two, then-by-six counter. Its principle function is to control the secondary scan gate A4. The divide-by-twelve is used only for IRIG C, the divider being reset at the count of ten or by the sync input for the other codes. This early reset is shown on the timing diagram as A18-8. The reset pulse is quite short and therefore has been widened for clarity. The area between the dotted lines on Sheet two is simply eliminated when the divider resets at ten. Reset at ten is established by gate A18-8. A one-shot (A18-12,6) performs code frame reset. The external reset signal (pin Z) may be used for code frame reset when W1 is installed, or the card can supply a reset pulse to synchronize the associated accumulator when W2 is installed.

Divider A7 (if present) is a divide-by-five counter provided for external use. It is synchronized with the other divider chips.

3) SCAN GATES

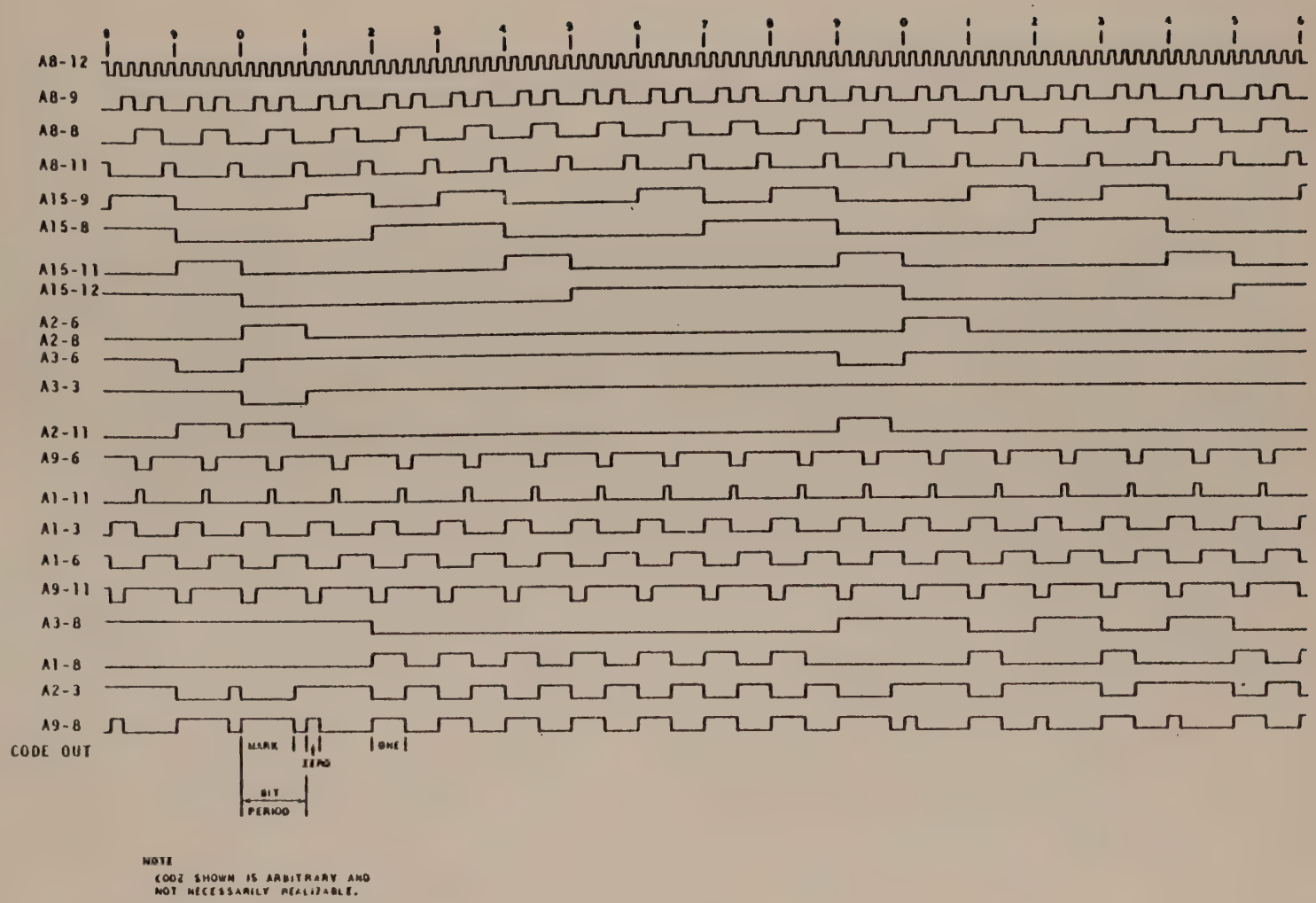
Creation of serial ONES is accomplished by a two-stage switching network and a series of gates. Chips A10-A14 are basically single pole (pin 8 is the output), 8-position switches. The inputs to these switches are the time data from the system accumulator. (One or more of these chips may be deleted on a particular card configuration.) The switching is controlled by BCD information on pins 1, 2 and 13. Since the above switches have the BCD inputs in parallel, all the time decades will provide outputs simultaneously; thus, the need for

switch A4. This switch, controlled from the BCD outputs of divider A17, selects the proper time interval for serializing each switch output. (The series of gates associated with A14 and A13, if present, further control these switches which may have outputs that should not be present in certain codes.) For example, tenths-of-seconds are added only in IRIG A, units-of-seconds are deleted in IRIG E, and all seconds information is deleted in IRIG C. Gates A3-8, A3-11 and A3-8 are used to inhibit the presence of serials ONES at certain times when no serial ONES should be present. This prevents the spurious ONES (coming from the switches) from appearing in the output code.

4) CODE GENERATING GATES

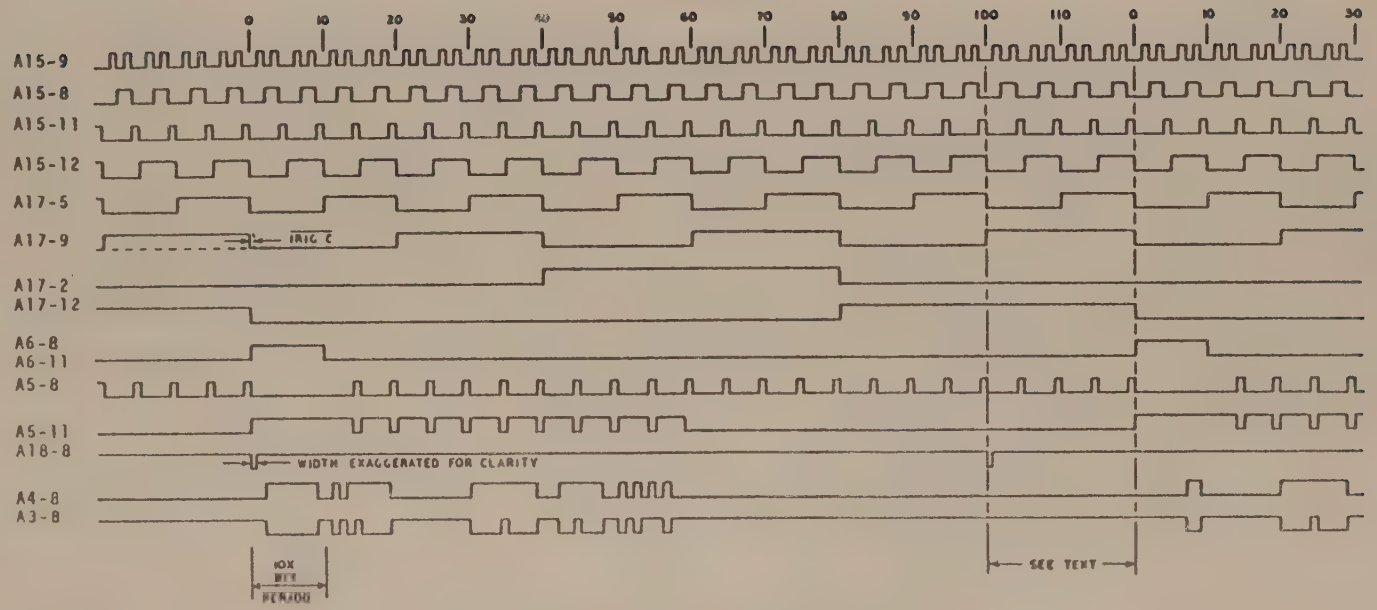
These gates must generate three time intervals in a 2:5:8 ratio. The time for the intervals is dependent on the bit period and is determined by the "Z RATE" on pin 2. A "2" length is a ZERO, a "5" is a ONE, and an "8" is an INDEX MARKER.

The INDEX MARKERS are generated by gating the output of divider A15. Gate A1-3 adds information from the output of divider A11 to create the "8" width. Gates A6-8 and A6-11 allow an extra pulse from gates A2-6 and A2-8 to give the "double mark" at the start of the frame. Gate A3-6 provides the marker at each tenth frame interval. Gate A9-11 supplies a pulse of "2" width at the start of each bit interval. If a MARKER or a ONE is not present, then the output code will be high for only the "2" width. Gate A1-6 supplies the "5" width pulse. This is AND-gated with the $\overline{\text{SERIAL ONES}}$ from A3-8 by gate A1-8. (External bits may be inserted on this same line through pin 22.) The presence of a ONE will cause the "5" width to appear in the output code, masking the "2" width which is always present. Gates A2-3 and A9-8 are used to combine the various widths to produce the output code at pin B.



NOTE
CODE SHOWN IS ARBITRARY AND NOT NECESSARILY REALIZABLE.

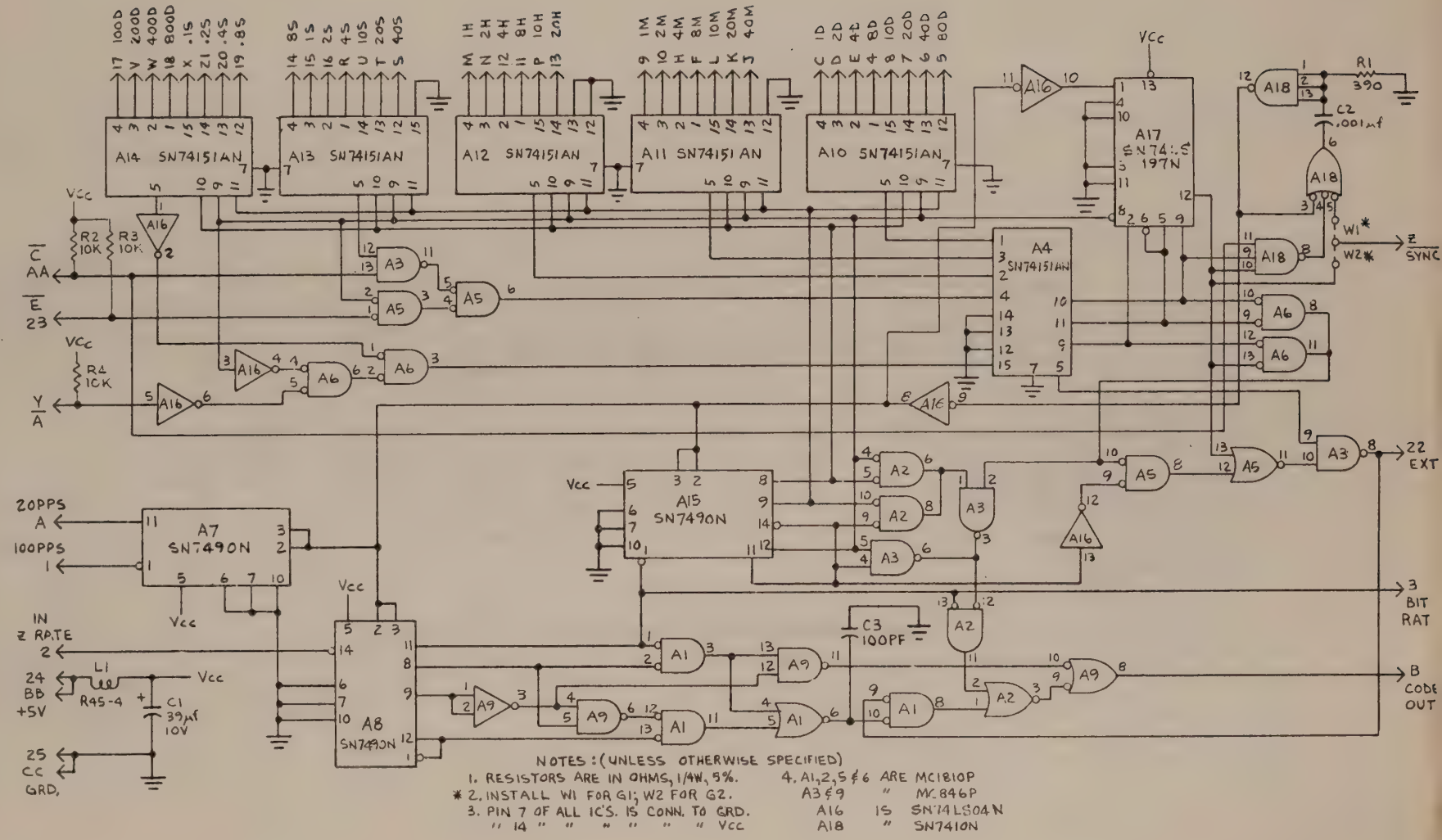
IRIG DC CODE GENERATOR - TIMING DIAGRAM - (Sheet 1 of 2)



NOTES:
CODE SHOWN (SERIAL ONES & A18-8) IS ARBITRARY AND NOT NECESSARILY REALIZABLE.

IRIG DC CODE GENERATOR - TIMING DIAGRAM - (Sheet 2 of 2)

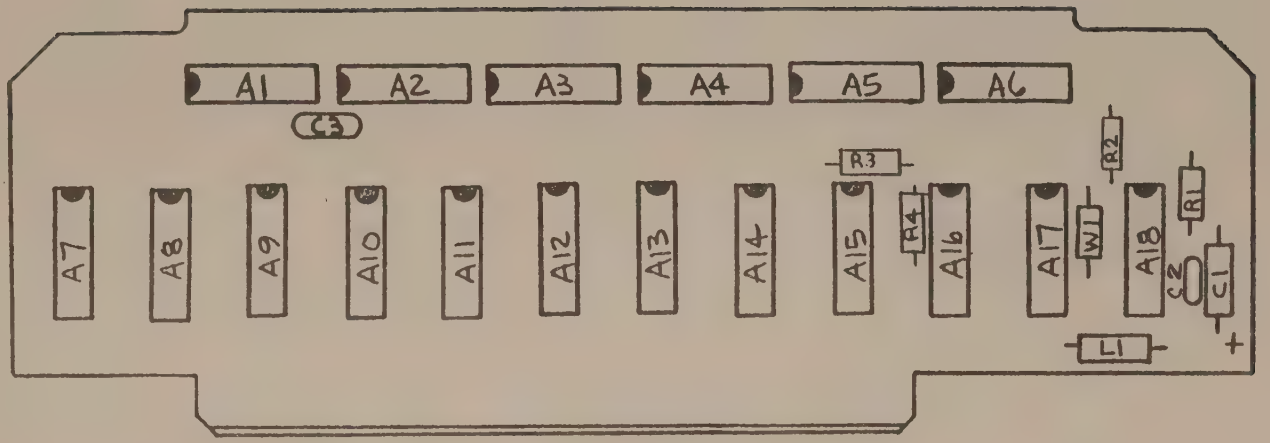
021554-7-1



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE IN OHMS, 1/4W, 5%.
* 2. INSTALL W1 FOR G1; W2 FOR G2.
3. PIN 7 OF ALL IC'S. IS CONN. TO GRD.
" 14 " " " " " " Vcc
4. A1,2,5 & 6 ARE MC1810P
A3 & 9 " MC846P
A16 IS SN74LS04N
A18 " SN7410N

CODE GENERATOR SCHEMATIC #021554-7-1



CODE GENERATOR ASSEMBLY #021554-4-1 REV E

PARTS LIST
CODE GENERATOR #021554-7-1 REV E

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly	021554-4-1
	Schematic	021554-7-1
A1,2,5,6	Integrated Ckt, MC1810P	025735
A3,9	Integrated Ckt, MC846P	019716
A4,10-14	Integrated Ckt, 74151	02577101
A7,8,15	Integrated Ckt, 7490	025732
A16	Integrated Ckt, 74LS04	103749
A17	Integrated Ckt, 74LS197	103165
A18	Integrated Ckt, 7410	019706
C1	Capacitor, 39 µF, 10V	100183
C2	Capacitor, .001 µF	100076
C3	Capacitor, 100 pF, DM15	100173
L1	Inductor, R45-4	101313
R1	Resistor, 390Ω ¼w 5%	101592
R2-4	Resistor, 10K ¼w 5%	101570
W1	Jumper, Molded	102879
	Extractor	100865

CIRCUIT DESCRIPTION
AGC/CYCLE DETECTOR
SCHEMATIC #021569-7-1

1) GENERAL

The AGC/Cycle Detector card contains two separate and independent circuits. The first circuit (AGC) provides automatic gain control for the incoming signal. The second circuit (Cycle Detector) generates three control signals: Upper Large Cycle, Lower Large Cycle, and Each Cycle.

2) AGC

Serial time-code input (from the tape unit, or other source), pin 19, is applied to a voltage divider network which consists of R12 and FET Q1. The bias on the gate of Q1 determines the ratio of the divider network and therefore the signal level at the gate of Q2. Q2 is a source follower providing high input impedance (so as not to load the divider network) and low impedance to drive differential amplifier A5. The input to A5 is applied to the "+" input (pin 3) via C10 for noninverting operation, as applicable to the particular circuit configuration).

A5 is provided with negative feedback through R20 for a maximum gain of about 40dB, and two "roll-off" networks C13-R22, and C12 to ensure stability. Pins T, Y, and A are normally connected by an external jumper. When optional filter networks are used, they are connected between pins T and Y.

The amplified signal is applied to the base of Q4 which controls the emitter voltage of Q3. Q4 and Q3 form a signal peak-detection circuit which provides the AGC control voltage to the gate of Q1. The output on pin T is set from 2 to 2.5 V p-p through the AGC potentiometer R4.

3) CYCLE DETECTOR

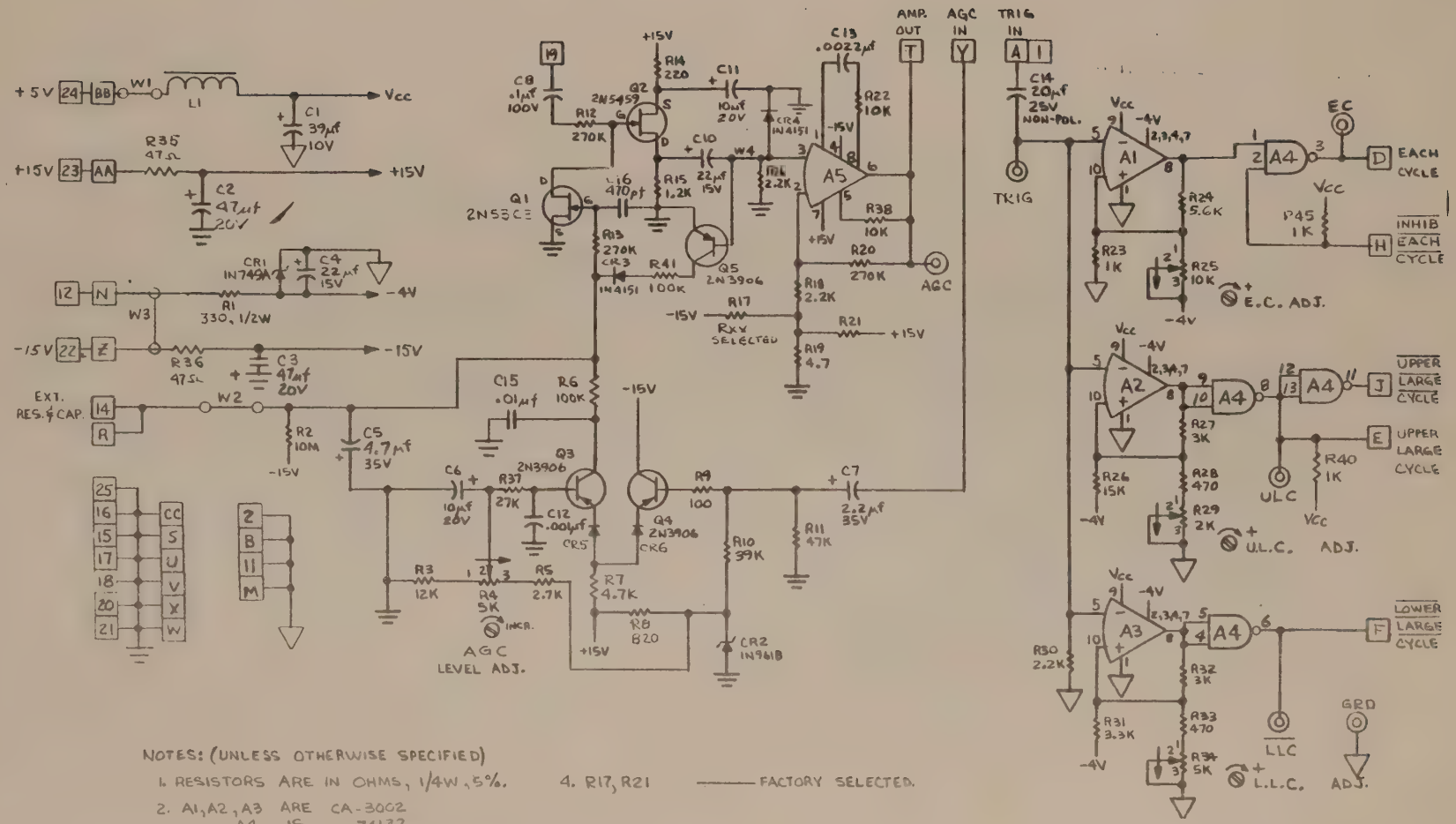
The output of amplifier A5 is also applied to three cycle-detector circuits, A1, A2 and A3.

A1 triggers at the zero-axis crossing and will generate a square wave at the input carrier frequency. The hysteresis of this trigger circuit is adjustable by means of the EC ADJ. potentiometer, R25.

A2 and A3 generate output pulses only upon receipt of a Large Half Cycle; A2, the Upper Large Cycle and A3 the Lower Large Cycle.

These two amplifiers will initiate their signals when the input signal reaches about 75% of the Large Half Cycle amplitude and will terminate them when the input signal reaches zero. The trigger points are adjustable by means of the ULC ADJ. and LLC ADJ. potentiometers, R29 and R34.

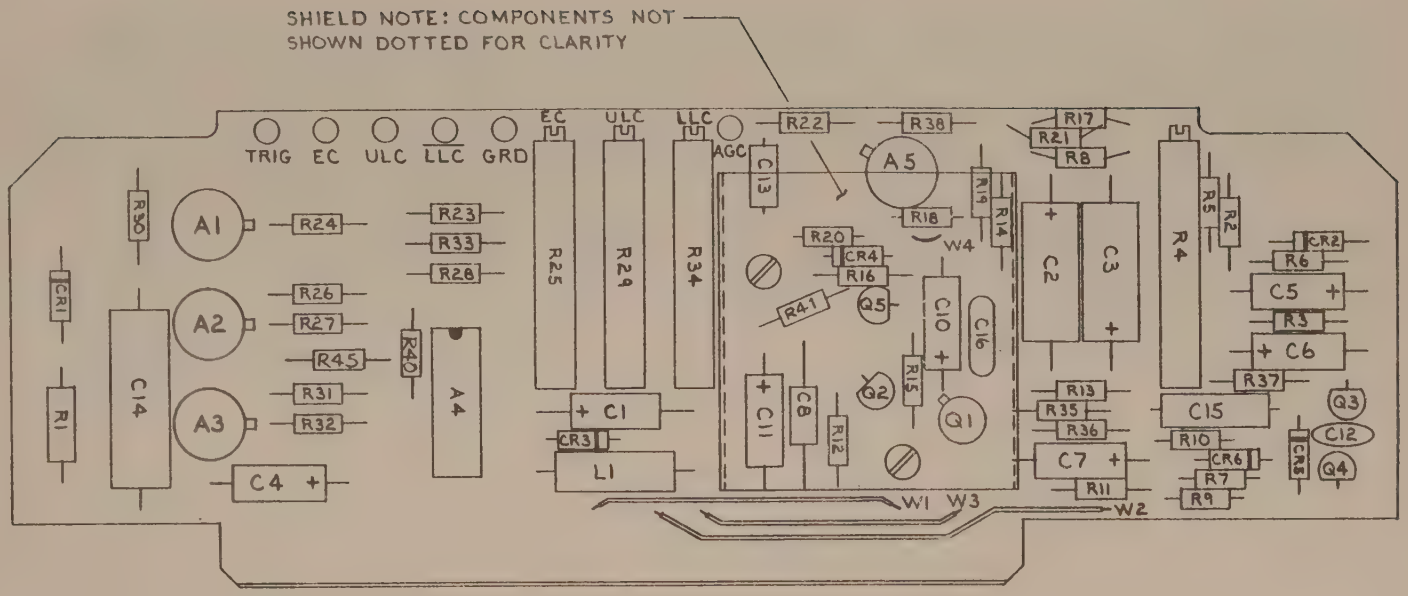
Saturating logic amplifiers, A4-2, A4-4, and A4-6, serve to amplify, invert the signals, and to provide isolation. A4-8 and A4-12 are used to inhibit the EC output when the $\overline{\text{INH EC}}$ (pin H) is grounded.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE IN OHMS, 1/4W, 5%.
2. A1, A2, A3 ARE CA-3002
   A4 IS 74132
   A5 IS 1439
3. PIN 14 OF A4 IS CONNECTED TO Vcc
   " 7 " " " " GRD.
4. R17, R21 ——— FACTORY SELECTED.

AGC & CYCLE DETECTOR SCHEMATIC #021569-7-1 REV U



AGC & CYCLE DETECTOR ASSEMBLY #021569-4-1 REV Q

PARTS LIST

AGC & CYCLE DETECTOR #021569-7-1 REV W

REF.	DESCRIPTION	SD PART NO.
	Assembly	021569-4-1
	Schematic	021569-7-1
A1-3	Integrated Circuit, CA3002	025701
A4	Integrated Circuit, 74132	045270
A5	Integrated Circuit, MC1439	025729
C1	Capacitor, 39 µF, 10 V	100183
C2,3	Capacitor, 47 µF, 20 V	100186
C4,10	Capacitor, 22 µF, 15 V	100125
C5	Capacitor, 4.7 µF, 35 V	100071
C6,11	Capacitor, 10 µF, 20 V	100063
C7	Capacitor, 2.2 µF, 35 V	100100
C8	Capacitor, .1 µF, 100 V	[illegible]0141
C12	Capacitor, 1000 pF, Disc	[illegible]
C13	Capacitor, .0022 µF	[illegible]
C14	Capacitor, 20 µF, 25 V, Tant	100264
C15	Capacitor, .01 µF, 200 V, Mylar	100168
C16	Capacitor, 470 pF, Mica	[illegible]
CR1	Diode, 1N749A	100419
CR2	Diode, 1N961B	100395
CR3-6	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
Q1	Transistor, 2N5363	101403
Q2	Transistor, 2N5459	101384
Q3-5	Transistor, 2N3906	101397
R1	Resistor, 330 Ω 5%, 1/2 W	10147402
R2	Resistor, 10 M 5%, 1/4 W	10156402
R3	Resistor, 12 k 5%, 1/4 W	10156502
R4,34	Potentiometer, 5 k, Beckman 78P	101938
R5	Resistor, 2.7 k 5%, 1/4 W	10159902
R6,41	Resistor, 100 k 5%, 1/4 W	[illegible]55802
R7	Resistor, 4.7 k 5%, 1/4 W	10159802
R8	Resistor, 820 Ω 5%, 1/4 W	10156702
R9	Resistor, 100 Ω 5%, 1/4 W	10160902
R10	Resistor, 39 k 5%, 1/4 W	10156102
R11	Resistor, 47 k 5%, 1/4 W	10157302
R12,13,20	Resistor, 270 k 5%, 1/4 W	10176902
R14	Resistor, 220 Ω 5%, 1/4 W	10156602
R15	Resistor, 1.2 k 5%, 1/4 W	10158102
R16,18,30	Resistor, 2.2 k 5%, 1/4 W	10156202

PARTS LIST

AGC & CYCLE DETECTOR #021569-7-1 (Cont'd)

REF.	DESCRIPTION	SD PART NO.
R19	Resistor, 4.7 Ω 5%, 1/4 W	10179602
R22,38	Resistor, 10 k 5%, 1/4 W	10157002
R23,40	Resistor, 1 k 5%, 1/4 W	10156902
R24	Resistor, 5.6 k 5%, 1/4 W	10158402
R25	Potentiometer, 10 k, Beckman 78P	101918
R26	Resistor, 15 k 5%, 1/4 W	10155202
R27,32	Resistor, 3 k 5%, 1/4 W	10154802
R28,33	Resistor, 470 Ω 5%, 1/4 W	10162502
R29	Potentiometer, 2 k, Beckman 78P	101876
R31	Resistor, 3.3 k 5%, 1/4 W	10155902
R35,36	Resistor, 47 Ω 5%, 1/4 W	10156002
R37	Resistor, 27 k 5%, 1/4 W	10158702
	Extractor	100865

CIRCUIT DESCRIPTION
READER LOGIC
SCHEMATIC #21588-7-3

1) GENERAL

Signals, $\overline{LLC}$ and EC respectively, are connected to pins A and 1 of the Reader Logic Card. The Reader Logic circuit accepts the EC and $\overline{LLC}$ signals and detects the ONES, ZEROS, and MARKS in the code. These signals are used to shift the BCD time information of the input code into a shift register and then transfer it to the Time-of-Day Accumulator Card which drives the Display drivers and Code Generator.

2) FUNCTIONAL

The basic scheme is as follows:

When a MARK is detected, the nine-bit shift register (A14) and 1/2 (A13) is cleared and a ONE set in the first bit position. Also, the "Y" counter A10 is advanced one.

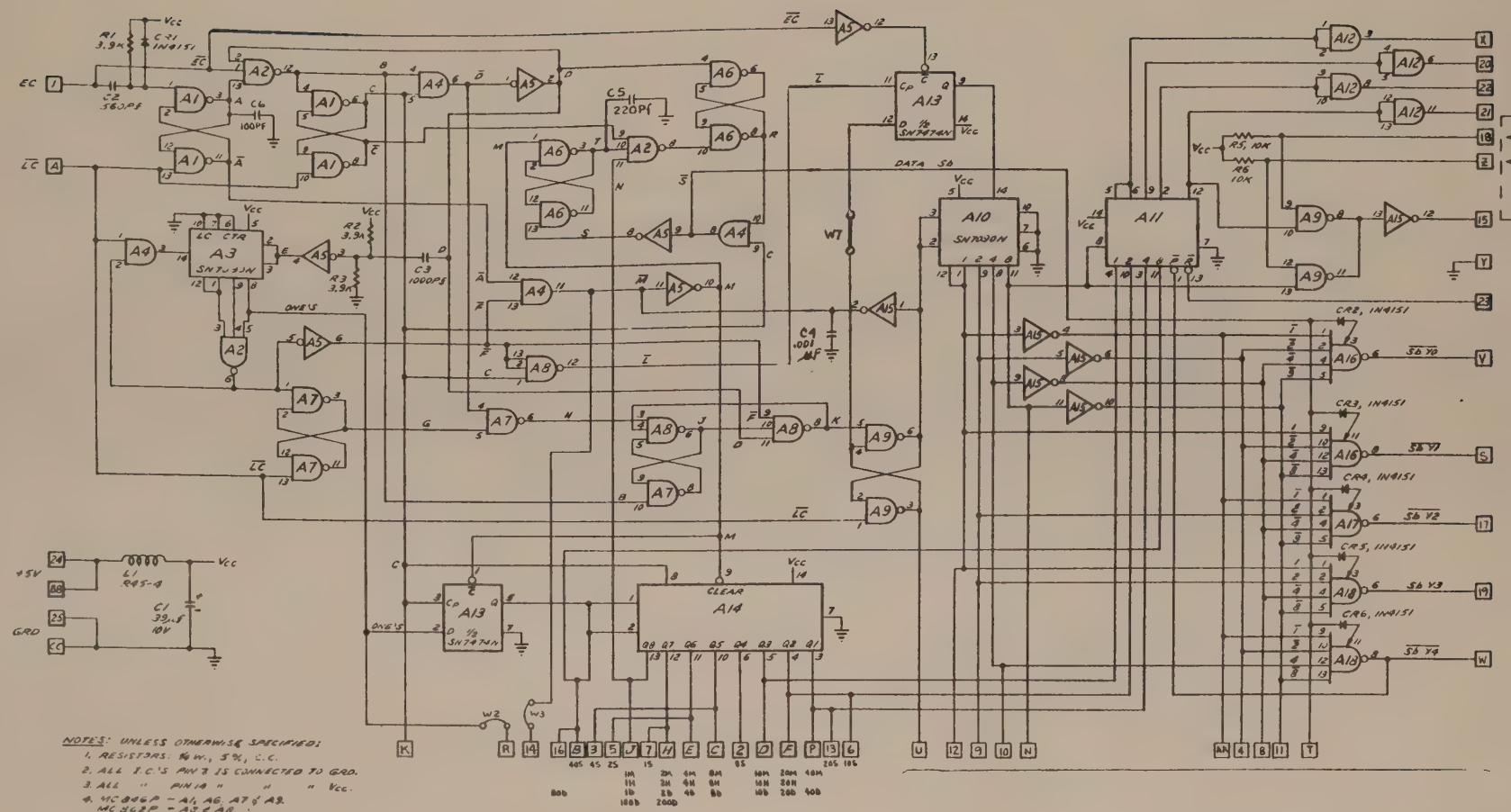
When the second MARK of the double MARK is detected, the sequence is changed so that the "Y" counter is set to ZERO if it was not already at ZERO. It is not advanced for this MARK. Nor is the shift register cleared. However, the ONE that was entered by the first MARK is shifted one position. The shift register is now advanced one position for each binary bit of the time frame. When the ONE that was entered by the first MARK reaches the ninth position, a circuit is set which permits the next shift signal to transfer the information from the register to the seconds section of the Time-of-Day Accumulator.

When the next MARK is detected, the register is cleared, a ONE entered and the "Y" counter advanced one. After nine bits are shifted into the register the information is transferred to the minutes section of the Accumulator. This cycle of operation is repeated a third time for hours information. If Days Option E20 is included, two additional cycles transfer this information to the Days Accumulator. The "Y" counter continues to count MARKS throughout the time frame.

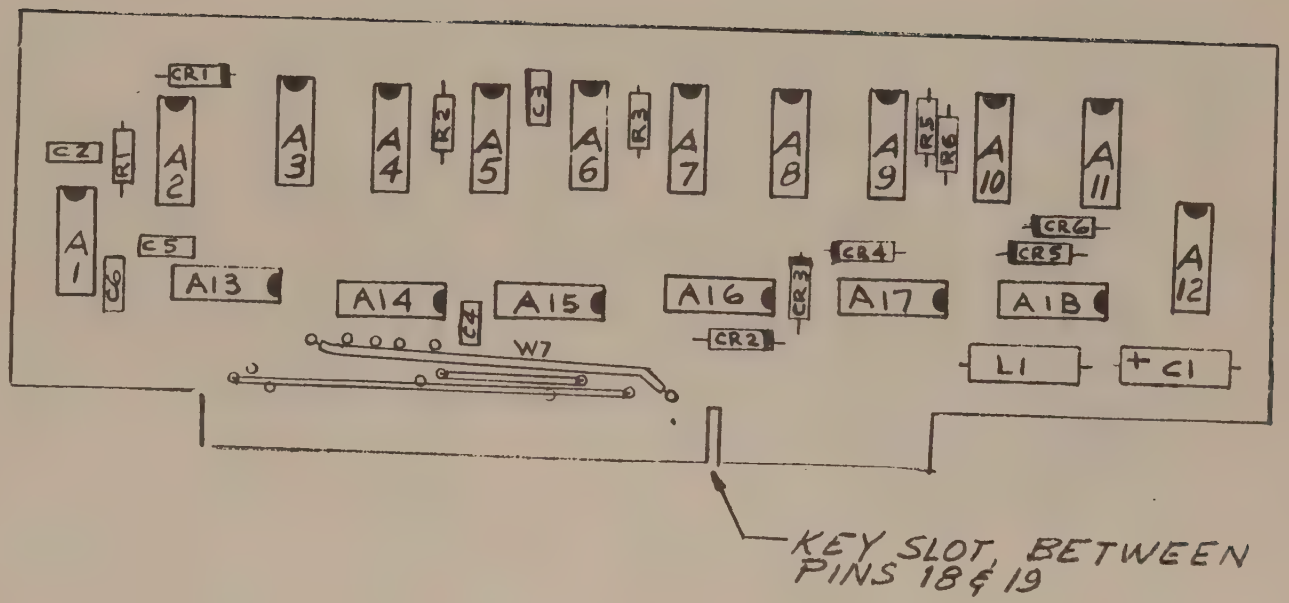
When the first MARK of the next double MARK is detected, it steps the "Y" counter from 9 to zero advancing the Time-of-Day Accumulator one second. It is thus updated at the beginning of the frame and will contain the same information (assuming no errors) scanned in during the frame.

The readout does not change during scan-in since the Accumulator is already updated.

The serial level shift code at pin R is fed to the Error Bypass circuit where it is compared with the output from the Code Generator which represents, in serial form, the contents of the Time Accumulator.


NOTES: UNLESS OTHERWISE SPECIFIED:
1. RESISTORS: ¼W., 5%, C.C.
2. ALL I.C.'S PIN 7 IS CONNECTED TO GRD.
3. ALL " PIN 14 " " " Vcc.
4. MC8096P - A1, A6, A7 & A9.
MC3628P - A3 & A8.
MC1806P - A4 & A12.
MC3206P - A5 & A15.
MC830P - A16, A17 & A18.
5. 74LS196 - A11
74164N - A14

READER LOGIC SCHEMATIC #D21588-7-3 REV E



READER LOGIC ASSEMBLY #A21588-4-3

PARTS LIST

READER LOGIC #021588-7-3 REV C

REF.	DESCRIPTION	SD PART NO.
	Assembly	021588-4-3
	Schematic	021588-7-3
A1,6,7,9	Integrated Circuit, MC846P	019716
A2,8	Integrated Circuit, MC862P	019719
A3,10	Integrated Circuit, SN7090N	025732
A4,12	Integrated Circuit, MC1806P	025733
A5,15	Integrated Circuit, MC836P	025704
A11	Integrated Circuit, SN74LS196N	103164
A13	Integrated Circuit, SN7474N	025241
A14	Integrated Circuit, SN74164N	025751
A16,17,18	Integrated Circuit, MC830P	019712
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 560 pF, Mica	100222
C3	Capacitor, .001 µF, DM15	100243
C4	Capacitor, 1000 pF, Disc	100076
C5	Capacitor, 220 pF, DM15	100220
C6	Capacitor, 100 pF	100173
CR1-6	Diode, 1N4151	100385
L1	Inductor	101313
R1-3	Resistor, 3.9 k 5%, 1/4 W, CC	10160102
R5,6	Resistor, 10 k 5%, 1/4 W, CC	10157002
W2,3,7	Wire, Insulated, 24GA	
	Extractor	100865

CIRCUIT DESCRIPTION
FWD/REV CONTROL
SCHEMATIC #021625-7-1

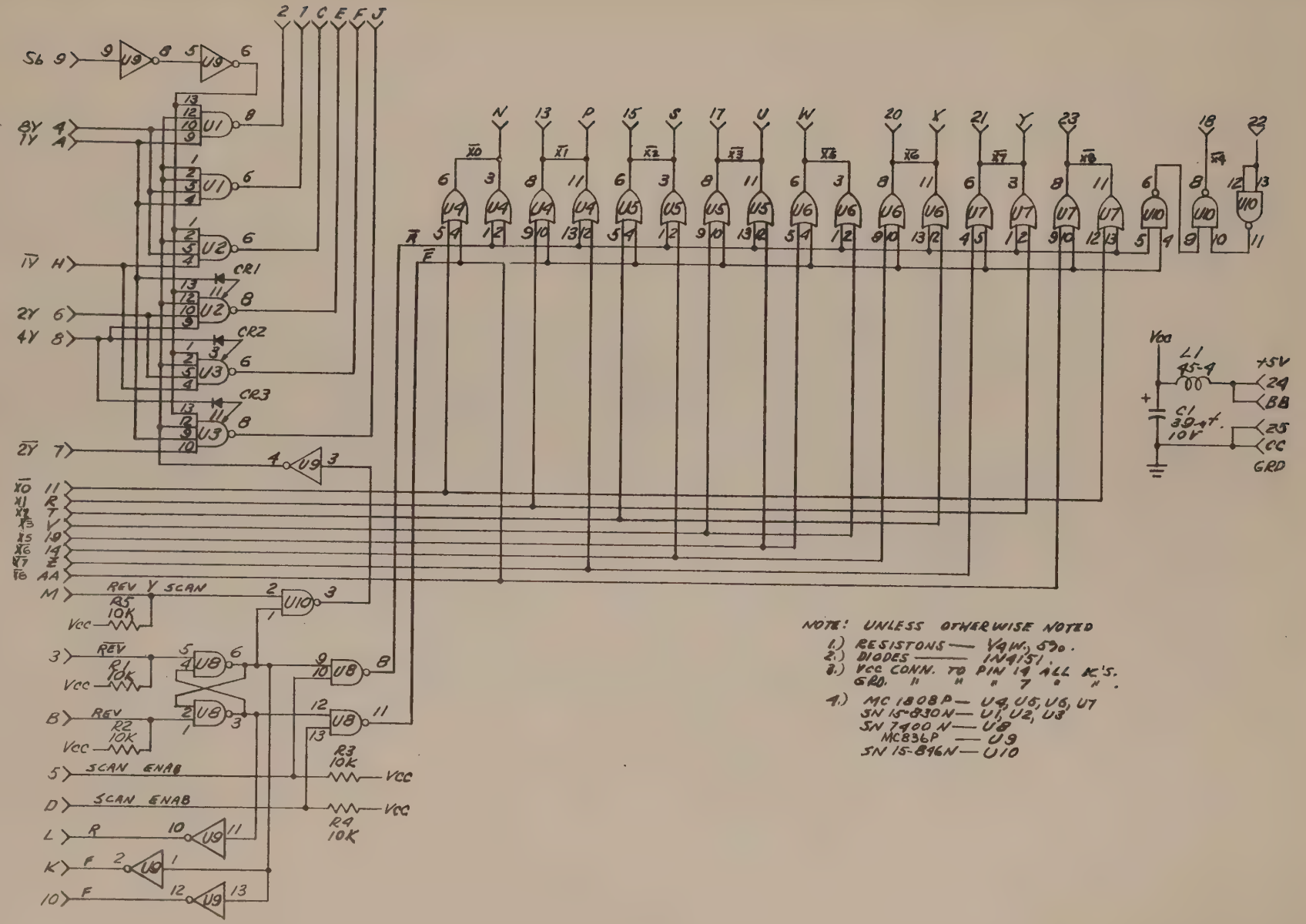
1) GENERAL

The FWD/REV Control Card, A13 contains gates which invert the order of the time data bits stripped from the input code when reading a reverse code. In addition, it provides buffered forward and reverse control signals and establishes the Y-Strobe signals needed to load data into the Time Accumulator when operating with a reverse code. This circuitry is active only when operating in one of the search modes. All circuits are disabled in the PRESET and GEN Modes.

2) OPERATION

Referring to Schematic #021625-7-1, the FWD and REV signals from the Tape Search section are fed to pins 3 and B, respectively. When operating in reverse (tape transport moving in a reverse direction) the FWD (REV) signal is at ground, and the $\overline{\text{REV}}$ signal is positive. Flip-flop U8-6/3 is set. The positive output from U8-6 is fed to 4 circuits: 1) through U10-3 and U9-4, opening Y Strobe Scan gates U1,U2 and U3; 2) through U8-8, opening gates U4-3, U4-11, U5-3, U5-11, U6-3, U6-11, U7-3 and U7-11 to negative time data signals $\overline{\text{X0}}$ through $\overline{\text{X8}}$; 3) through U9-2 to the Error Bypass circuit, disabling forward Y Scan; and 4) through U9-12, clamping the Z-Rate signal at ground, thus blocking update of the TOD Accumulator (A15) and inhibiting operation of the Code Generator A17) and Modulator (A8) circuits. The Y Strobe Scan gates load the rearranged data bits into the TOD Accumulator (A15) as each frame is stripped from the input code.

When forward operation is established, flip-flop U8-6/3 is reset. The Y Strobe Scan gates are disabled (all outputs driven positive), gates U4-6, U4-8, U5-6, U5-8, U6-6, U6-8, U7-6 and U7-8 are open (time data restored to normal order); U9-12 and U9-2 outputs are up, restoring normal operation of the TOD Accumulator, Code Generator, Modulator and Error Bypass circuitry.



FWD/REV CONTROL SCHEMATIC #C21625-7-1A

FWD/REV CONTROL ASSEMBLY #A21625-4-1A

PARTS LIST

RWD/REV CONTROL #021625-7-1 REV A_1

REF.	DESCRIPTION	SD PART NO.
	Assembly	021625-4-1
	Schematic	021625-7-1
C1	Capacitor, 39 µF, 10 V	100183
CR1-3	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
R1-5	Resistor, 10 k 5%, 1/4 W	101570
U1-3	Integrated Circuit, SN15830N	019712
U4-7	Integrated Circuit, MC1808P	025734
U8	Integrated Circuit, SN7400N	019705
U9	Integrated Circuit, MC836P	025704
U10	Integrated Circuit, SN15846N	019716
	Extractor	100865

CIRCUIT DESCRIPTION
MINOR COUNTER
SCHEMATIC #21632-7-2

1) GENERAL

The Minor Counter card can provide up to three serial decades with common reset, parallel preset and two sets of buffered, parallel BCD outputs. Provision is made to gate one set of BCD outputs in three 4-bit bytes. The input may be either ac or dc-coupled and fed to the first decade through an update inhibit circuit. Provision is included for three output pulse rates with 10% duty cycle which may be supplied in place of the days recycle circuit.

2) DECADE DIVIDERS

The up to three decade dividers are connected in tandum. Each is provided with parallel BCD data inputs which may be used to load preset information when the associated data strobe ($\overline{\text{PRESET}}$) line is grounded. Jumpers W1 and W2 permit the data strobe associated with the center decade (A4) to be wired in common with the data strobe input to the first decade (A1) or the third (A6). The decade zero-reset inputs are wired in common through buffers on A8 to pin 23. The parallel BCD outputs from each decade are wired to output pins through two sets of buffers.

3) OUTPUT BUFFERS

The BCD output buffers may be inverting or noninverting. One of the two sets (A10,A13 and A15) can be gated by inputs through pin L,K and J, respectively. These gate lines are buffered by inverters on A11.

4) INPUT INHIBIT CIRCUIT

This circuit allows the presence of a ground on pin H to inhibit input signals on pin F from updating the accumulator. Gate A2-6 inverts and buffers the input. Gates A2-11 and A2-8 form an RS flip-flip.

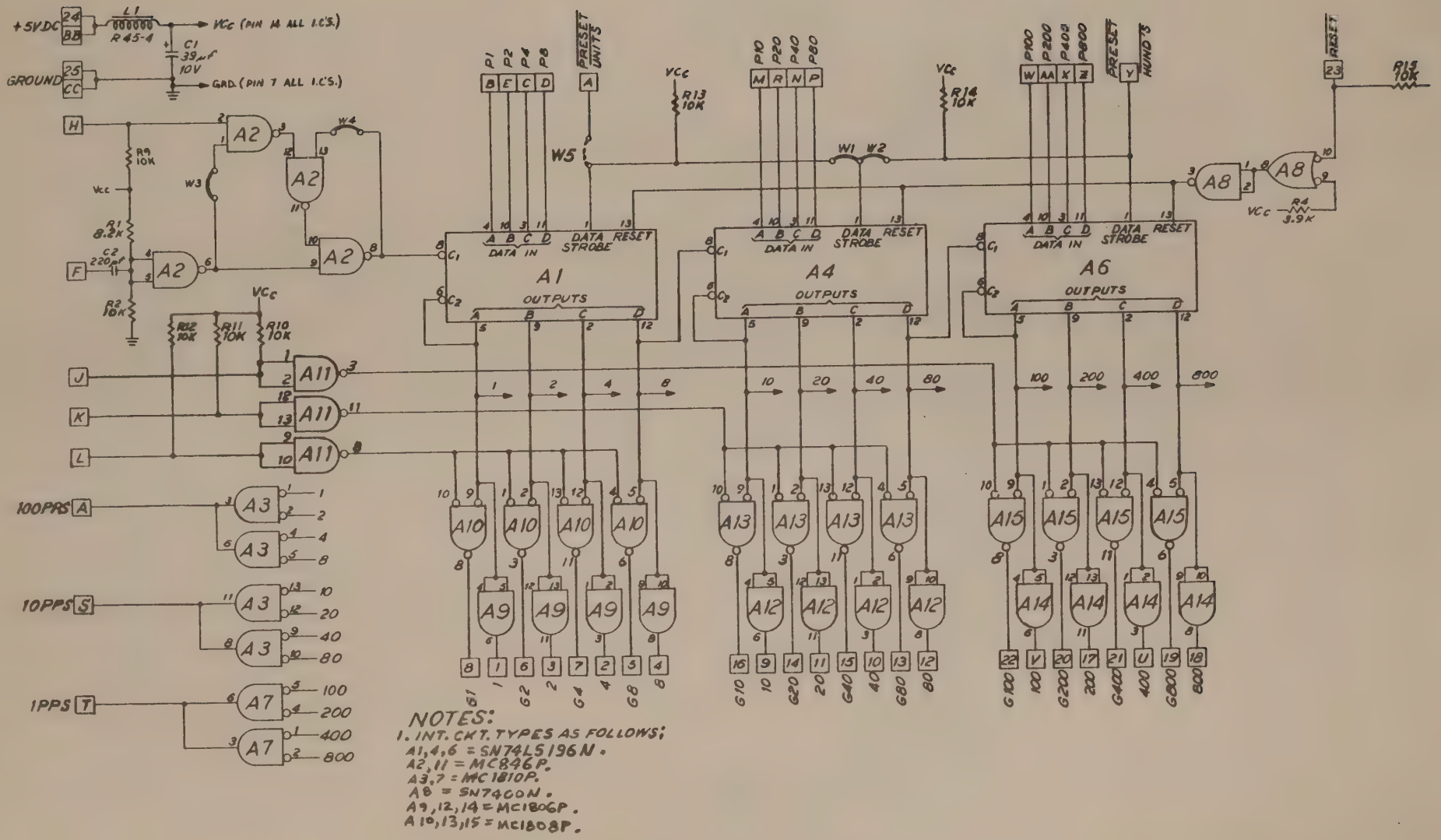
A2-3 gates the $\overline{\text{INHIBIT}}$ line and the inverted input. When the accumulator is updating, flip-flop A2-8,11 output follows the input. When the $\overline{\text{INHIBIT}}$ line, pin H, is grounded the flip-flop will latch with the output high. The output will go low the first time the input is low after the ground has been removed from the $\overline{\text{INHIBIT}}$ line.

5) OUTPUT PULSE RATES

Three sets of gates are used to produce three 10% duty cycle pulse rates. Each pulse goes high when the four outputs from the corres-

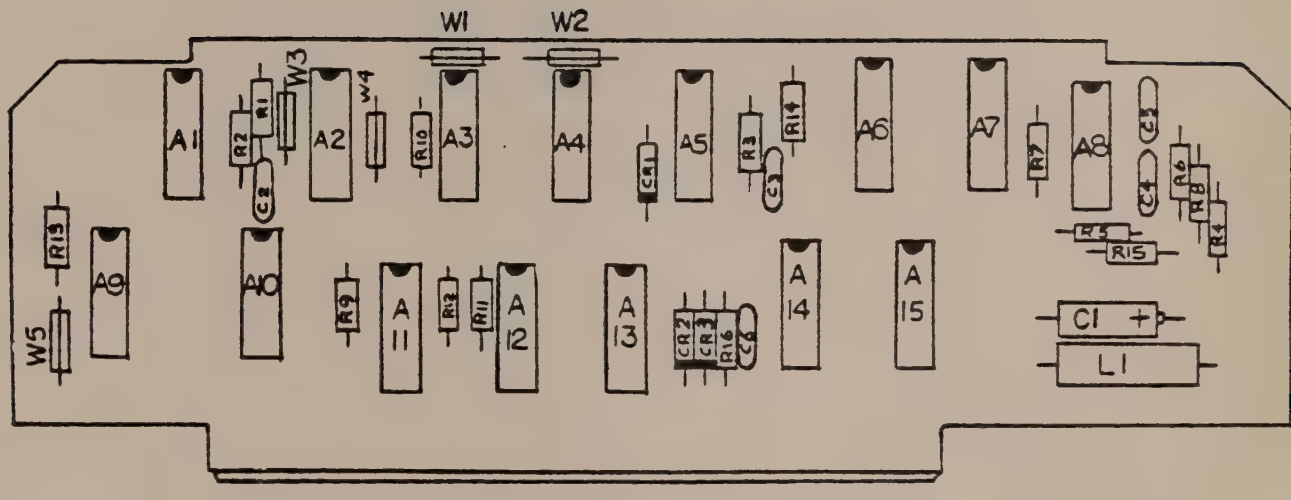
ponding decades are low (leading edge on time). The pulse remains up until the output of the decade in 001. Thus, the pulse is high 10% of the time. The output is a 5 V logic level behind 6 kΩ.

The pulse rate outputs are fed to pins A, S and T which are used for units preset and days recycle inputs on other configurations of the card. Chip A5 is removed when the rate outputs are supplied.



NOTES:
1. INT. CKT. TYPES AS FOLLOWS;
A1,4,6 = SN74LS196N.
A2,11 = MC846P.
A3,7 = MC1810P.
A8 = SN7400N.
A9,12,14 = MC1806P.
A10,13,15 = MC1808P.

3 DIGIT ACCUMULATOR BUFFER SCHEMATIC #021632-7-2 REV C



DAYS ACCUMULATOR ASSEMBLY #021632-4-1 REV C

PARTS LIST

MINOR COUNTER #021632-7-2 REV E_1

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly	021632-4-1
	Schematic	021632-7-2
A1,4,6	Integrated Ckt, 74LS196	103164
A2,11	Integrated Ckt, MC846P	019716
A3,7	Integrated Ckt, MC1810P	025735
A8	Integrated Ckt, 7400	019705
A9,12,14	Integrated Ckt, MC1806P	025733
A10,13,15	Integrated Ckt, MC1808P	025734
C1	Capacitor, 39 µF, 10V	100183
C2	Capacitor, 220 pF, DM	100220
L1	Inductor, R45-4	101313
R1	Resistor, 8.2K ¼w 5%	10159502
R2,9,10-15	Resistor, 10K ¼w 5%	10157002
R4	Resistor, 3.9K ¼w 5%	10160102
W1-W4	Jumper, Molded	102879

CIRCUIT DESCRIPTION
PRESET AND ERROR BYPASS
SCHEMATIC #7-05153802

1) GENERAL

This card contains Preset Control, Error Bypass, Pulse Rate, Z-Rate, FWD/REV, and Reset circuits. It is used in the Model 8132 Reader, the Model 8134 Reader/Search Unit, the Model 8152 Generator/Reader and the Model 8154 Generator/Reader/Serach unit.

2) OPERATION

PRESET CONTROL: Referring to the lower right corner of the schematic, Preset Logic is provided for detecting TOD and Days Coincidence in the Model 8154 Time Code Generator/Reader/Search Unit. When armed in the PRESET Mode, these circuits combined with the comparator, detect coincidence between the time entered on the front panel PRESET/START TIME thumbwheel switches and the contents of the accumulator. The coincidence signals are sent to preset control circuits on Time Base & Control Card A27. When Days/ID Option E13 is included, these circuits separate the Days and TOD sections of the comparator providing separate Days and TOD Coincidence outputs to Card A27.

ERROR BYPASS: The Error Bypass circuit is shown at the top of the schematic. It is enabled in the READ Forward Mode of Operation only and includes provision for selecting 0,3,5,7 or 9 frames of Error Bypass. This means that data stripped from the input code will not be loaded into the Accumulator until after the selected number of consecutive error frames has been counted. (READ Reverse is equivalent to "0" error bypass in which all data are loaded into the Accumulator irrespective of errors.)

The Error Bypass circuit accepts the serial level shift output from the Reader Logic Card and compares it with the serial level shift output from the Code Generator Card in exclusive OR gate U13-11. The output from this gate is fed to gate U7-6 along with blanking and sampling signals which differ as a function of the code being read and the options present in the Reader.

The sampling signal from U14-2 is developed in Counter/Decoder U1/U2 from the Z-Rate input and selected by U3. It is a pulse at Z4 time for IRIG and NASA Codes and at Z5 time for XR3 Code.

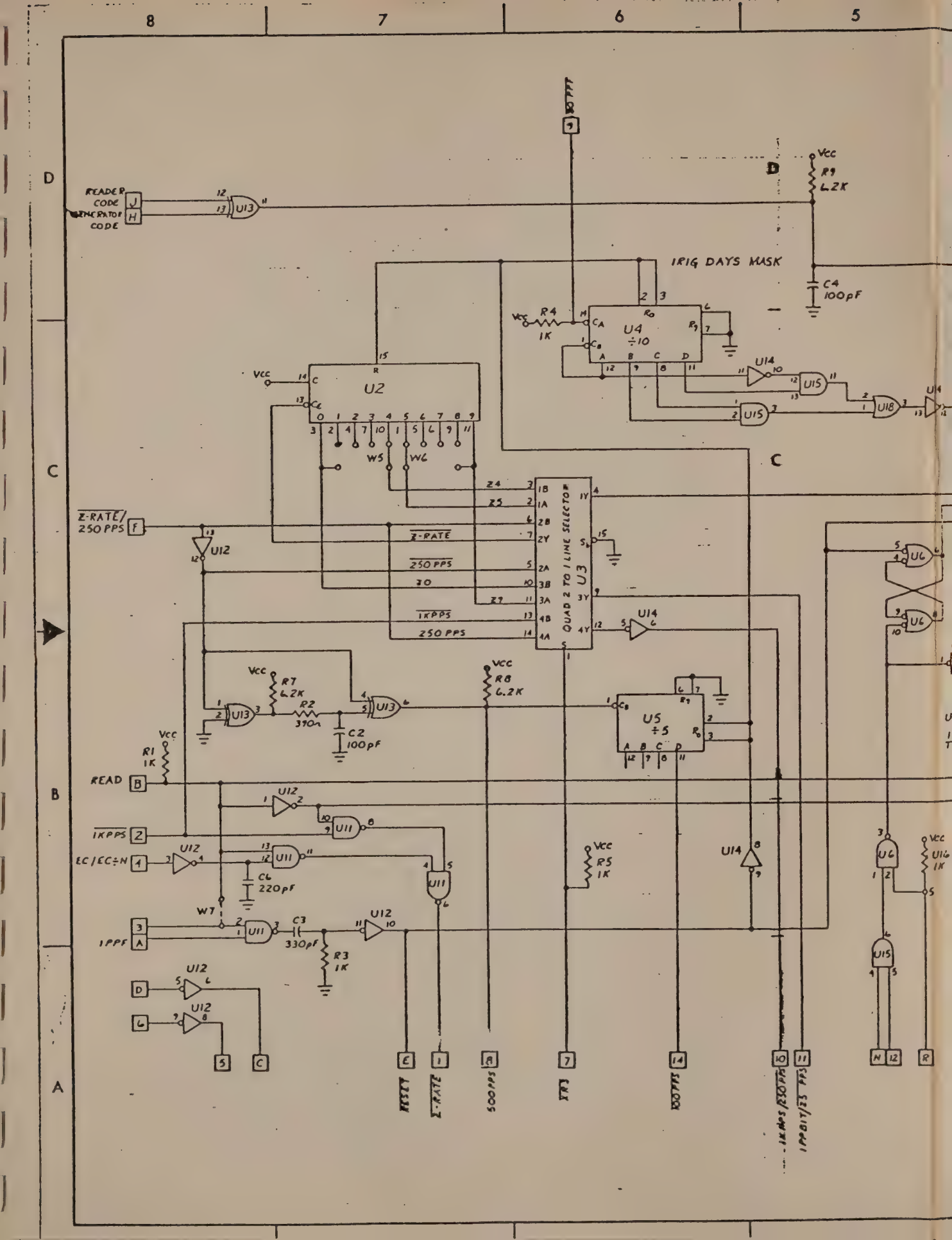
The IRIG Days Mask from U14-12 is developed by Counter U4 and associated decoding gates from the 20 ppF input to pin 9. It inhibits comparison of days bits so that readers without the Days Option can read IRIG Codes containing days.

The blanking signal from flip-flop U6-6, 8 restricts comparison to that portion of the code containing time information. It is set by the differentiated leading edge of the 1 ppF input through U11-3, C3, U12-10 ($\overline{\text{RESET}}$), and cleared by the output from the 3 input NAND gate formed from U15-6 and U6-3. The $\overline{\text{RESET}}$ signal clears flip-flop U10-3/U6-11, provided it was set by the detection of at least one error (U7-6 output going low) during the previous frame. Assuming that no error has occured, this flip-flop will not be set and output U6-11 will be high opening gate U10-6. When the cl clear signal from U6-3 occures during the current frams, it is inverted by U19-2 and fed through U10-6 resetting counter U9 and flip-flop U7-8/U10-8. The low output from U7-8 is fed through U20-3 and U20-8 to pin 23 and the Reader Logic Card, inhibiting forward Y-Scan. (Gates U20-3, 8 are open in READ Forward only.) This same

signal is fed through U20-11 to pin 20. The resulting output is used to enable the comparators in tape search units. Now, if an error occurs during the next frame, flip-flop U10-3/U6-11 will be set (with U10-3 high and U6-11 low) and, when U6-3 output goes low during the frame, U10-6 will be closed and counter U9 will not be reset. The $\overline{\text{RESET}}$ signal at the start of the next frame clears flip-flop U10-3/U6-11 and counter U9 accumulates one count. If the next frame is good, U9 is reset and the count starts over. If the next frame is bad, however, U9 accumulatoes a second count. The BCD outputs from counter U9 are decoded by U8 and fed to a set input to flip-flop U7-8/U10-8 through gates on U17 which are used to select the desired number of error bypass frames. When counter U9 reaches this number, flip-flop U7-8/U10-8 is set enabling forward scan of the time data (stripped from the input code by the Reader Logic during the next frame) into the Accumulator. The tape search comparators, when present, are inhibited by the output from U20-11 during this one frame. Counter U9 is reset through U19-4 and U10-11 and the sequence starts again. The selected number of consecutive error frames must occur before the input time data is permitted to be loaded into the Accumulator.

PULSE RATES: Selected pulse rates from U3 through U14-4 and U14-6 and from edge detector U13-3,6 and counter U5 are provided as outputs when XR3 Time Codes are being read.

Z-RATE and RESET: These circuits, shown at the lower left on the schematic, select Z-Rate output for GENERATE and READ and develope a $\overline{\text{RESET}}$ pulse from the leading edge of the 1 ppF input.


8
7
6
5
D
C
B
A
READER CODE
ENCRYPTOR CODE
U13
Vcc
R9
4.2K
IRIG DAYS MASK
C4
100pF
R4
1K
U4
÷10
U2
U14
U15
U18
W5
W6
Z-RATE/
250 PPS
U12
Z-RATE
250 PPS
30
1KPPS
250 PPS
U3
QUAD 2 TO 1 LINE SELECTOR
R7
4.2K
R2
390Ω
C2
100pF
R8
6.2K
U5
÷5
R1
1K
READ
1KPPS
EC/EC÷N
C6
220pF
W7
1PPF
C3
330pF
R3
1K
R5
1K
U6
U16
U11
1KBIT/SEC
1KBIT/2SEC

REVISIONS				
REV	DESCRIPTION	ENG NO	ECO NO	DATE
B	CHG'D IC'S, R3,4,C3; ADD'D R7-16.		17167	11/3/80 GM
C	REDESIGNED W/OUT U1 & U9.		17515	4/1/81
A	RELEASED TO ECO/NFC			
A,	DELETED W9; ADD'D W8. (ECR 019-79)		NFC	3/26/79

NOTES:
1. RESISTORS ARE ¼W, 5%, CARBON COMP
2. DIODES ARE IN4151
3. IC'S:

		Vcc	GND
U4,5	74LS390	5	10
U2, 8	14017	16	8
U3	74LS157	16	8
U6,10,11	74LS00	14	7
U7	74LS20	14	7
U12,14	74LS04	14	7
U13	74LS136	14	7
U15	74LS08	14	7
U16	BECKMAN 899-1-R1K	14	—
U17	74LS126	14	7
U18	74LS32	14	7
U19	74LS05	14	7
U20	74LS09	14	7

LIST OF MATERIALS

PROPRIETARY DATA
Furnished under United States Government Contract No. _____
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8154	
8152	
8134	
8132	
USED ON	NEXT ASSY
APPLICATION	

DRAWN JK 5-8-81 DATE
CHECK DATE
ELECT. DATE
MECH. DATE
PROJECT K DATE
DATE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMAL TOLERANCE
.X ±
.XX ±
.XXX ±
ANGLES ±

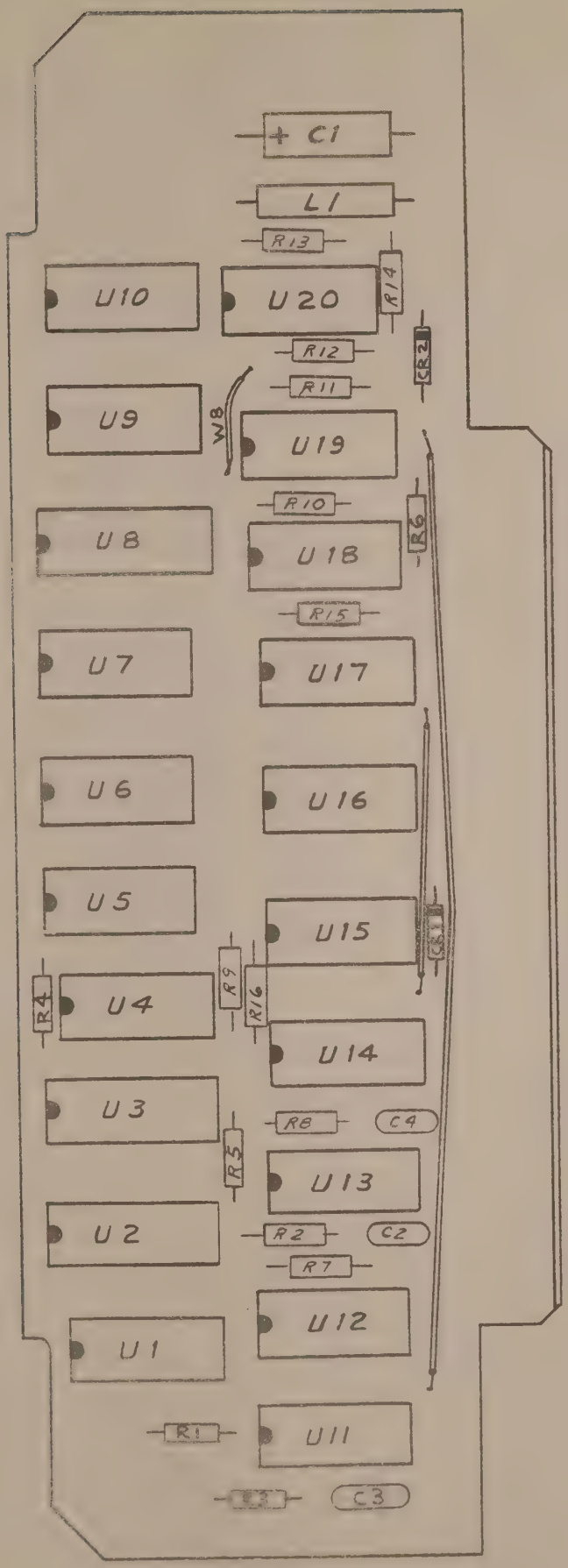
SCALE ∅ DO NOT SCALE DRAWING
SH 1 OF 1

STRATTON DONNER CORPORATION
CONCORD, CALIFORNIA
CODE IDENT. 52542

PRESET AND ERROR BYPASS

MATERIAL

DRAWING NO.
REF D SIZE 05153802 PART NO. REV C



PRESET/ERROR BYPASS ASSEMBLY #05153802 REV B

8132-5-81

PARTS LIST

PRESET AND ERROR BYPASS #05153802 REV B

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly	05153802
	Schematic	7-05153802
C1	Capacitor, 39µF, 10V	100183
C2,3	Capacitor, 100 pF	11762801
C4	Capacitor, 300 pF	11763601
CR1,2	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
R1, 3,4,5	Resistor, 1 K, ¼w 5%	10156901
R2	Resistor, 390Ω ¼w 5%	10159201
R6	Resistor, 270Ω ¼w 5%	10154201
R7-16	Resistor, 6.2K ¼w 5%	10160801
U1,4,5,9	Integrated Ckt, 74LS90	116554
U2,8	Integrated Ckt, 74LS42	103131
U3	Integrated Ckt, 74LS157	117249
U6,10,11	Integrated Ckt, 74LS00	103130
U7	Integrated Ckt, 74LS20	103969
U12,14	Integrated Ckt, 74LS04	103749
U13	Integrated Ckt, 74LS136	116923
U15	Integrated Ckt, 74LS08	103967
U16	1 K Resistor Pack	116454
U17	Integrated Ckt, 74LS125	116513
U18	Integrated Ckt, 74LS32	103972
U19	Integrated Ckt, 74LS05	116113
U20	Integrated Ckt, 74LS09	116925
	Extractor	100865

CIRCUIT DESCRIPTION
POWER SUPPLY
SCHEMATIC #041810-7-9

1) GENERAL

The power supply provides four regulated dc voltages (±5 V and ±15 V), five unregulated dc voltages (±9 V, ±21 V and +210 V), and an 18 V rms time base output at the line frequency. The regulated output voltage levels are adjustable. These outputs are current limited and are short-circuit-proof to ground. (Note: Overheating may result if a short is maintained over an extended period of time.) Both voltage-sense and sense-return lines are provided for the regulated outputs. These lines are wired to provide regulation at the load. Fuses are provided for the unregulated +21 V and +210 V on the power supply assembly.

Input power is 115/230 V, 48 to 440 Hz at less than 100 W with nominal line and all outputs fully loaded. (Note: The line frequency may be limited, 48 to 62 Hz unless Option L12 is utilized, by the fan characteristics if a fan is included in the unit.) Input power is fed to transformer T1 through line filter Z1, fuse F1, a front panel power switch and 115/230 select switch, S101. The third wire is grounded to the chassis.

The transformer is constructed with split-primary windings which are connected in parallel for 115 V operation and in series for 230 V operation. Selection is made by 115/230 switch, S101. (Note: Units are normally shipped in the 115 V configuration with a 2A Slo-Blo fuse, F1. If the unit is converted to 230 V operation, F1 should be changed to 1A Slo-Blo.) Three secondary windings (two with center taps) are provided, one for ±9 V, one for ±21 V and 18 V rms, and the third for +210 V.

2) NONREGULATED SUPPLIES

The +210 V nonregulated supply is developed by the bridge rectifier formed from diodes CR5 through CR8, plus the filter circuit formed from R1, R2 and C5. The resulting output is fed through F2 (0.125A) to P103, pins 18 and V. It is used to drive front panel numerical indicating tubes and is rated at 100 mA.

The ±21 V nonregulated supplies are developed by bridge rectifier CR1 through CR4 and filtered by C1, C2, C8 and C11. The +21 V output is used internally as the source for the +15 V regulator. It is fed through F3 (1A) to P103, pins 15 and S, where it is available for use as a relay supply. The -21 V output is used internally as the source for the -15 V regulator, and to power both the -15 V and -5 V regulator amplifiers. It is also available at P103, pin 4, for external use. Each of the ±21 V supplies is rated at 0.5A.

The 18 V rms is derived from the secondary winding which provides the ac voltage to develop the ±21 V. This rms voltage is fed through R15 to P103 pins 22 and Z.

The +9 V nonregulated supply is developed by full-wave rectifier CR11, CR12 and filtered by C3, C4 and C10. It is used internally as the source for the +5 V regulator, and to power both the -15 V and -5 V regulator amplifiers. It is available at P103, pins 21 and Y, for external use as a lamp supply. It is rated at 4A.

Tge -9 V nonregulated supply from full-wave rectifier CR9, CR10 and filter C6 is used internally as the source for the -5 V regulator. It is available at P103, pin 2, for external use. It is rated 0.5A.

3) REGULATED SUPPLIES

The regulated +15 V, 0.5A output at P103, pin N, is established through pass transistor Q1 under the control of regulator U1 and the divider network (R4, R5, R6) between the +15 V SENSE line (P103, pin 12) and ground. The voltage on the arm of 15 V ADJ potentiometer (R5) is fed to U1 where it is compared with the internal reference, referred to the 15 V sense-return line (P103, pin 8). The current limit is imposed by sensing the drop across R9 and the circuit is stabilized by network R32, C7.

The regulated -15 V, 0.5A output at P103, pin 5, is established through Q2 and Q3 under the control of regulator amplifier U3-12. It uses the +15 V SENSE line as the reference, comparing it with the output through R10, R11 and the -15 V supply.1 Potentiometer R5 serves as the adjustment for both outputs. Current is limited by cutting the base drive to Q2 when the drop across R14 approaches one diode drop.

The regulated +5 V, 4A output at P103, pins P and R, is established through Q4 and Q5 under the control of regulator U2 and a divider network (R18, R19). The +5 V SENSE line at P103, pins 13 and 14, is compared with the fraction of the U2 internal reference voltage appearing on the arm of 5 V ADJ potentiometer (R19). The current limit is imposed by sensing the drop across R24 through divider R22, R23. The circuit is stabilized by network R33, C12. The regulated -5 V, 0.5A output at P103, pin C, is established through Q6 and Q7 under the control of regulator amplifier U3-10. It uses the +5 V SENSE line as reference, comparing it with the output through R26, R27 and the -5 V SENSE line at P103, pin 3. The -5 V output tracks the +5 V supply and potentiometer R19 adjusts both. Output current is limited by cutting the base drive to Q6 when the drop across R30 approaches one diode drop.

4) CALIBRATION PROCEDURE

Test Equipment: see Chapter 4.

Check that fuse F1 is the proper size for the input voltage selected:

2 A, 115 V

1 A, 230 V

With an input of 115 V ac (230 V is so equipped) ±5%, 50/60 Hz.

Check the following at the Power Supply P.C. Board edge connector:

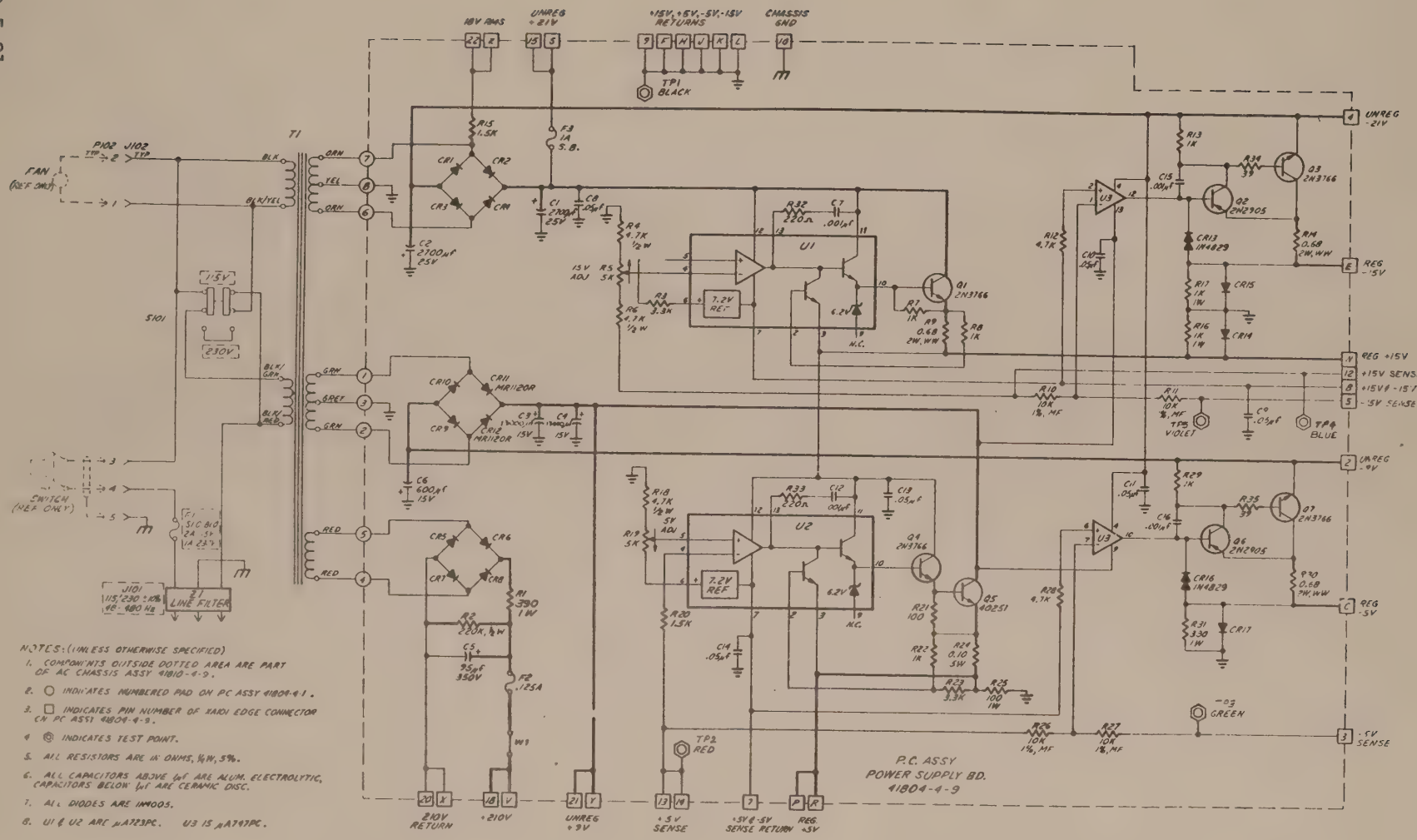
1) +210 V ±25% at pins V, 18 (GND 20, X)
2) +21 V ±20% at pins S, 15 (GND BLACK TEST POINT)
3) +9 V ±20% at pins Y, 21 (GND BLACK TEST POINT)
4) -9 V ±20% at pin 2 (GND BLACK TEST POINT)
5) -21 V ±20% at pin 4 (GND BLACK TEST POINT)

Measure the +15 V supply on the BLUE (GND BLACK) Test Point and adjust R5 (15 V ADJ) for +15 V ±0.3 V.

Measure the -15 V supply on the VIOLET Test Point and verify that it is within ±0.3 V of -15 V. Readjust R5 if necessary so that both +15 and -15 V supplies are within ±0.3 V.

Measure the +5 V supply on the RED Test Point and adjust R19 (5 V ADJ) for 5 V ±0.1 V.

Measure the -5 V supply on the GREEN Test Point and verify that it is within ±0.1 V of -5 V. Readjust R19 if necessary so that both +5 and -5 V supplies are within ±0.1 V.

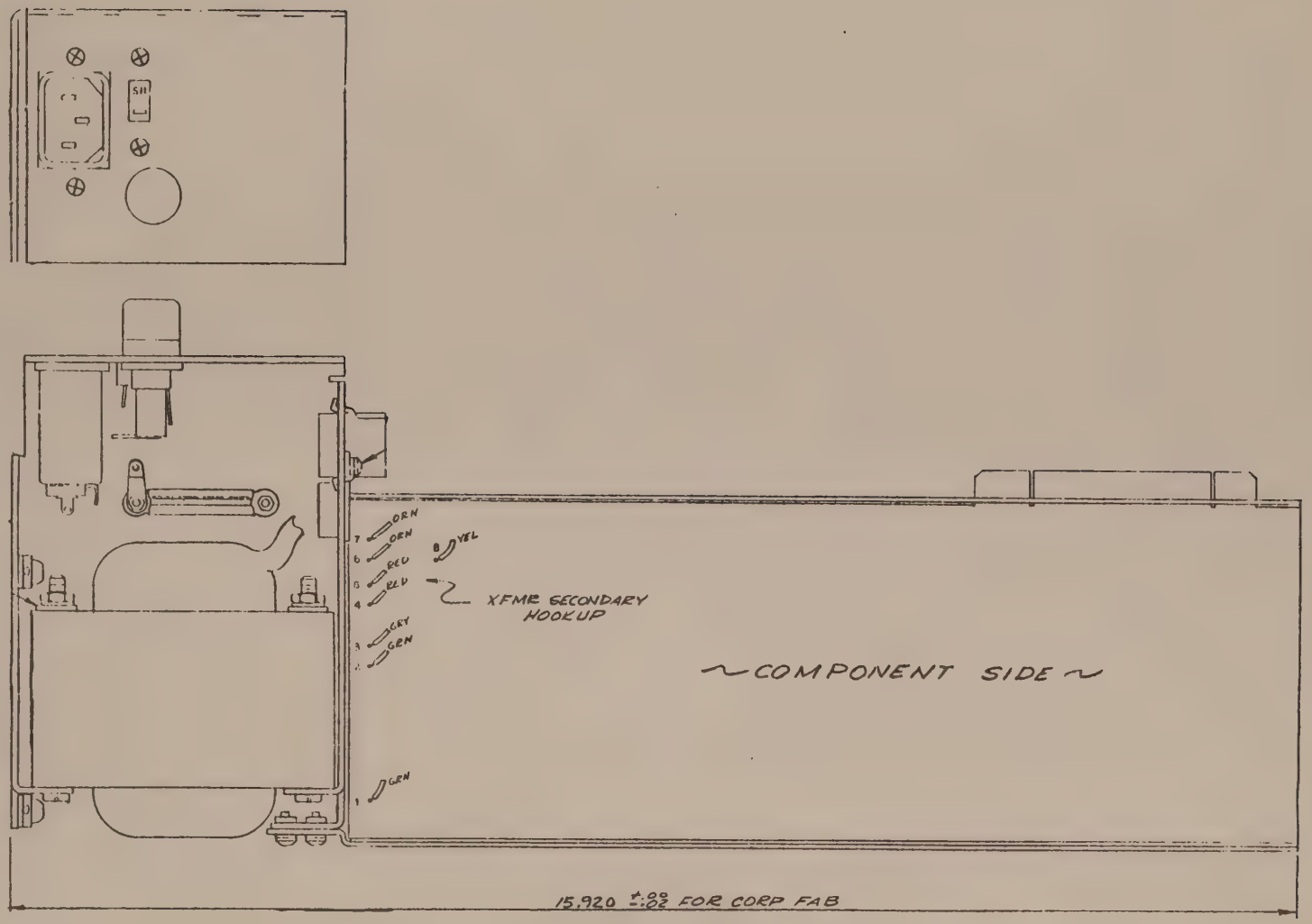


NOTES: (UNLESS OTHERWISE SPECIFIED)

1. COMPONENTS OUTSIDE DOTTED AREA ARE PART OF AC CHASSIS ASSY 41810-4-9.
2. ○ INDICATES NUMBERED PAD ON PC ASSY 41804-4-1.
3. □ INDICATES PIN NUMBER OF 22/44 EDGE CONNECTOR ON PC ASSY 41804-4-9.
4. ⬡ INDICATES TEST POINT.
5. ALL RESISTORS ARE IN OHMS, ½W, 5%.
6. ALL CAPACITORS ABOVE 1µF ARE ALUM. ELECTROLYTIC, CAPACITORS BELOW 1µF ARE CERAMIC DISC.
7. ALL DIODES ARE IN4005.
8. U1 & U2 ARE µA723PC. U3 IS µA747PC.

P.C. ASSY
POWER SUPPLY BD.
41804-4-9

POWER SUPPLY
SCHEMATIC #041810-7-9 REV C1

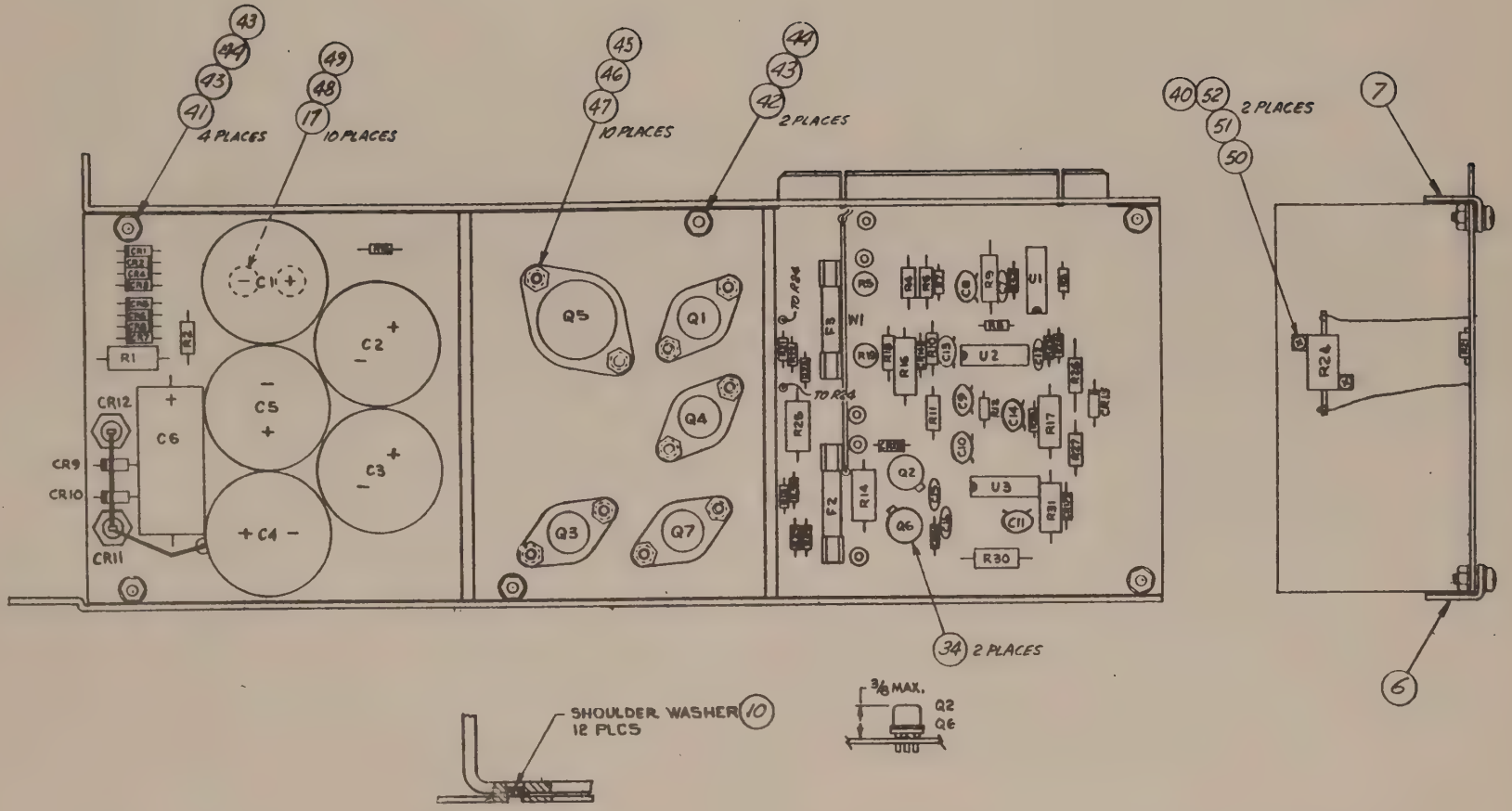


POWER SUPPLY ASSEMBLY #041810-4-9 REV A

PARTS LIST

POWER SUPPLY ASSEMBLY #041810-4-9 REV A_1

REF.	DESCRIPTION	SD PART NO.
	Assembly	041810-4-9
	Schematic	041810-7-9
	Assembly, Power Supply Board	041804-4-9
J101/Z1	Line Filter/Power Input	102461
J102	Connector Shell, 5 contacts	101264
F1	Fuse, 2A Slow-Blow, 115 V	100585
S101	Switch, Slide	102331
T1	Transformer	021408-6-1
XF1	Fuse, Post	102409
	Contact, Female (J102)	10282201
	4-40 x 7/16 PHMS	10062607
	4-40 x 1/4 PHMS	10062604
	#4 Flat Washer	100703
	#4 Kep Nut	100941
	Ground Lug	100486
	#10-32 x 2.75 PHMS	10064444
	#10 Fiber Washer	100684
	Grommet	100885
	4-point Terminal Strip	100084
	6-32 x 5/16 FHMS	10073105
	#6 Kep Nut	100862
	6-32 x ¼ PHMS	10063204
	#6 Split Lock Washer	100712
	Power Supply Cable	041810-3-6



POWER SUPPLY BOARD #041804-4-6 REV D

PARTS LIST

POWER SUPPLY BOARD #041804-4-9 REV F_2

REF.	DESCRIPTION	SD PART NO.
	Assembly	041804-4-9
	Schematic	041810-7-9
C1,2	Capacitor, 2700 µF, 25 V	100232
C3,4	Capacitor, 13,000 µF, 15 V	116074
C5	Capacitor, 95 µF, 350 V	100259
C6	Capacitor, 600 µF, 15 V	100258
C7,12,15,16	Capacitor, .001 µF, 1 kV, Disc	100076
C8-11,13,14	Capacitor, .05 µF, 50 V	100134
CR1-10,14,15,17	Diode, 1N4005	100413
CR13,16	Diode, 1N4829	100443
F2	Fuse, 3 AG .125 A Slow Blow	100592
F3	Fuse, 3 AG, 1 A A	100584
Q1,3,4,7	Transistor, 2N3766	101373
Q2,6	Transistor, 2N2905	101382
Q5	Transistor, 40251	101354
R1	Resistor, 390 k, 1 W, CC	101532
R2	Resistor, 220 k, ½ W, CC	101458
R3,23	Resistor, 3.3 k, ¼ W, CC	101559
R4,6,18	Resistor, 4.7 k, ½ W, CC	101511
R5,19	Potentiometer, 5 k	101859
R7,8,13,22,29	Resistor, 1 k, ¼ W, CC	101569
R9,14,30	Resistor, .68 Ω, 2 W, WW	101829
R10,11,26,27	Resistor, 10 k, 1/8W, MF	101930
R12,28	Resistor, 4.7 k, ¼ W, CC	101598
R15,20	Resistor, 1.5 k, ¼ W, CC	101577
R16,17	Resistor, 1 k, 1 W, CC	101635
R21	Resistor, 100 Ω, ¼ W, CC	101609
R24	Resistor, 0.1 Ω, 5 W, WW	102218
R25	Resistor, 100 Ω, 1 W, CC	101856
R31	Resistor, 330 Ω, 1 W, CC	101624
R32,33	Resistor, 220 Ω, ¼ W, CC	101566
R34,35	Resistor, 39 Ω, ¼ W, CC	101733
U1,2	Integrated Circuit, 723PC	025761
U3	Integrated Circuit, 747PC	045205
W1	Bare Wire	W-48
XF2,3	Socket, Fuse	116299
XQ1,3-5,7	Socket, Pin	102442
XU1-3	Socket, 14-pin	102433

PARTS LIST

POWER SUPPLY BOARD #041804-4-9 (Cont'd)

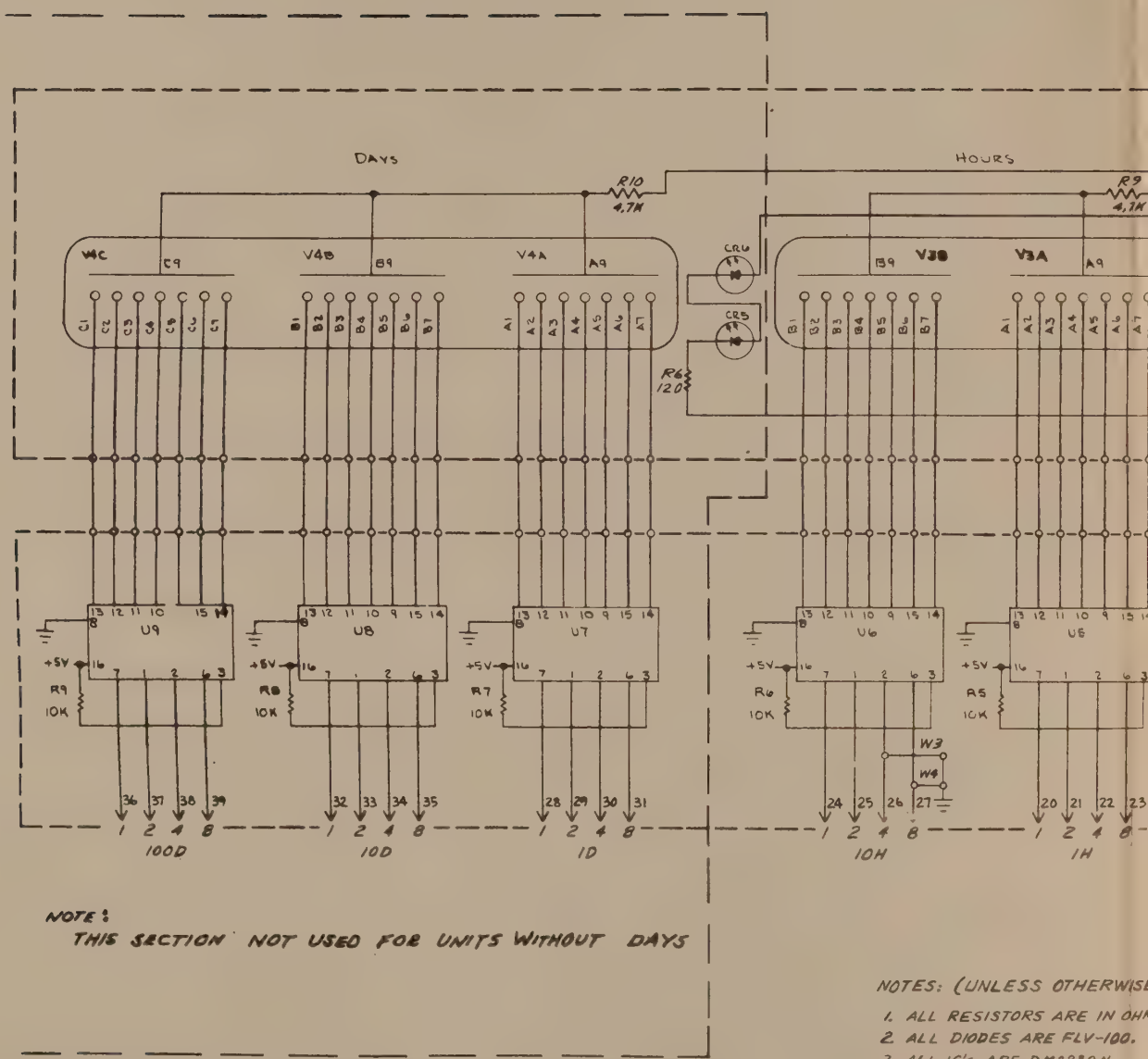
REF.	DESCRIPTION	SD PART NO.
	Test Point, Red, +5 V	100541
	Test Point, Black, Grd.	100542
	Test Point, Green, -5 V	100543
	Test Point, Blue, +15 V	100547
	Test Point, Violet, -15 V	100548
(Q2,Q6)	Socket, Pin	103037

CIRCUIT DESCRIPTION
DISPLAY ASSEMBLY
SCHEMATIC #041945-7 -2

1) GENERAL

The display assembly has one 3-digit and three 2-digit, in-line, planar indicator tubes and associated driver chips for the display of time in days, hours, minutes and seconds. LED colons are provided between the tubes. Time information is accepted in parallel BCD form. A voltage regulator is used to develop +180V from the +210V input for use by the display tubes.

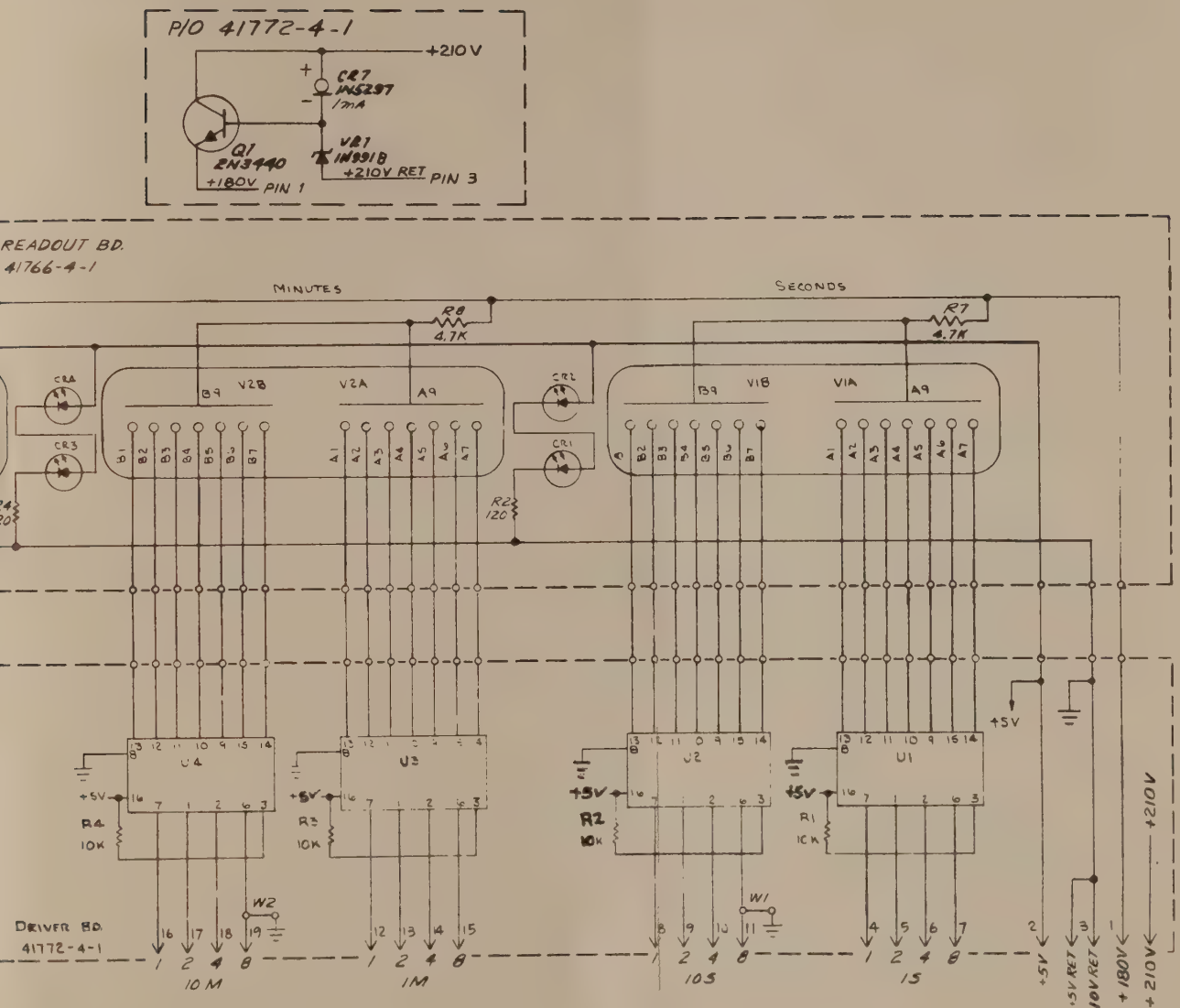
The Assembly Drawing 041945-4-7 is formed from two main subassemblies plus the voltage regulator as shown on the schematic. The Readout Board Assembly 041766-4-1 mounts the display tubes and LED colons. The Driver Board Assembly 041772-4-1 mounts the display drivers which convert the BCD input to the 7-line required by the display tubes. The two boards are interconnected by right-angle pin assemblies.



NOTES: (UNLESS OTHERWISE

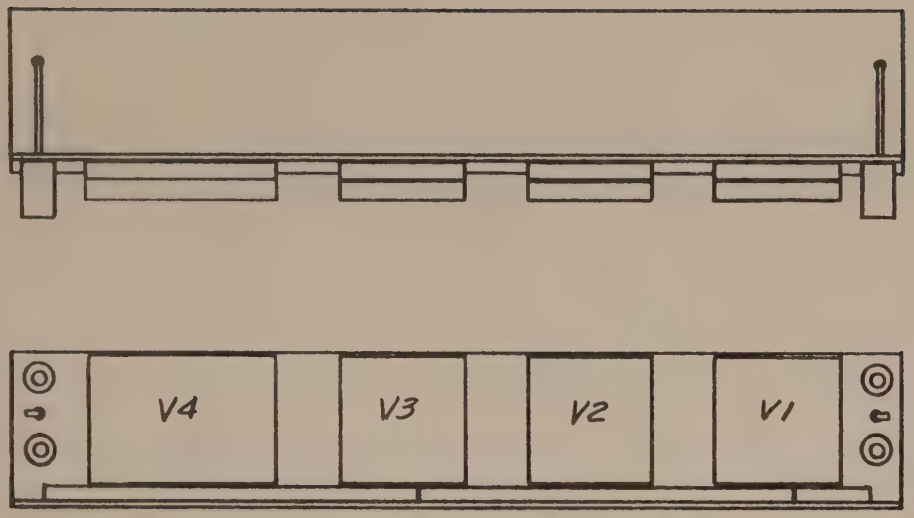
1. ALL RESISTORS ARE IN OHM
2. ALL DIODES ARE FLV-100.
3. ALL IC's ARE DM8880N

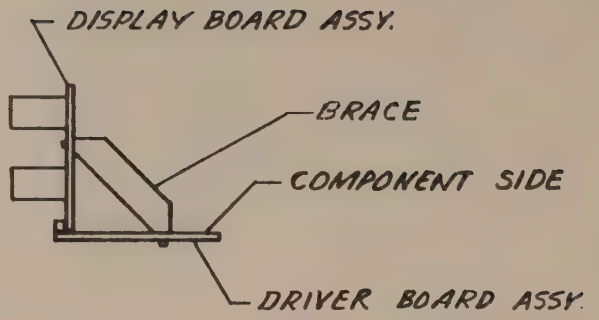
READ OUT AND DRIVER SCHEMA



SPECIFIED)

5, ¼W, 5%.



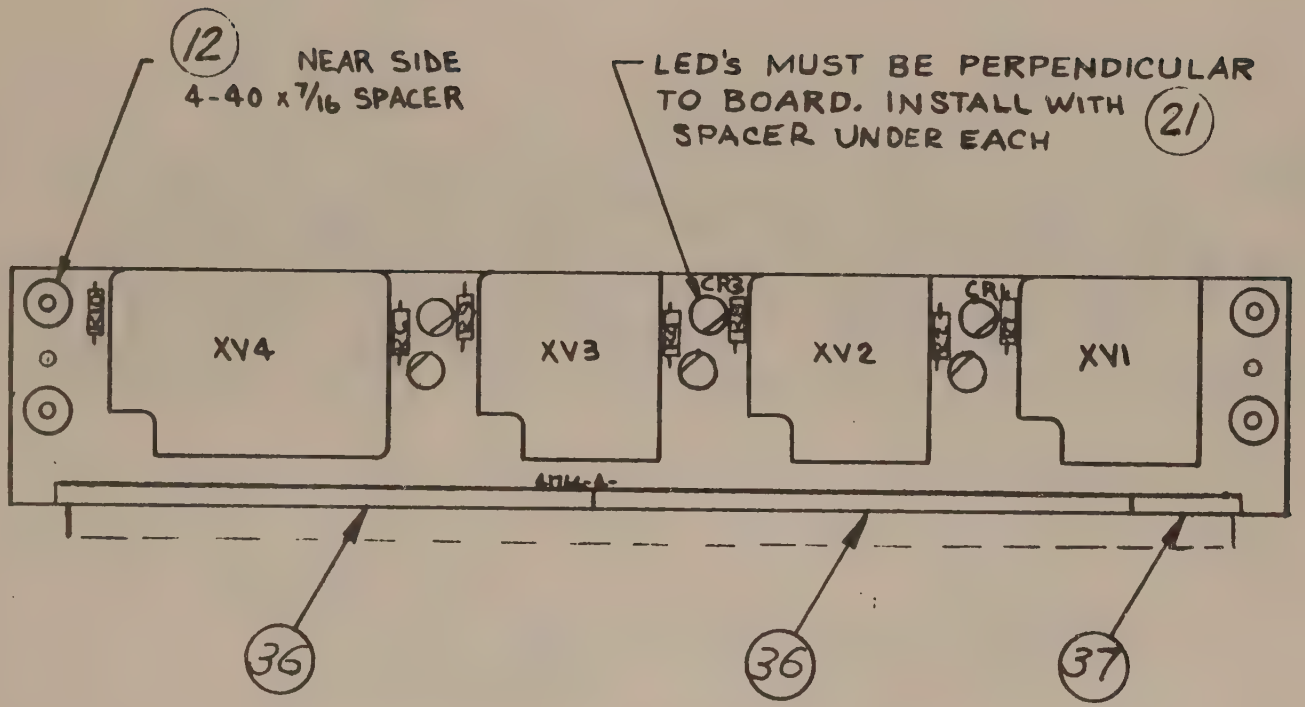


9 DIGIT DISPLAY ASSEMBLY #041945-4-7 REV B

PARTS LIST

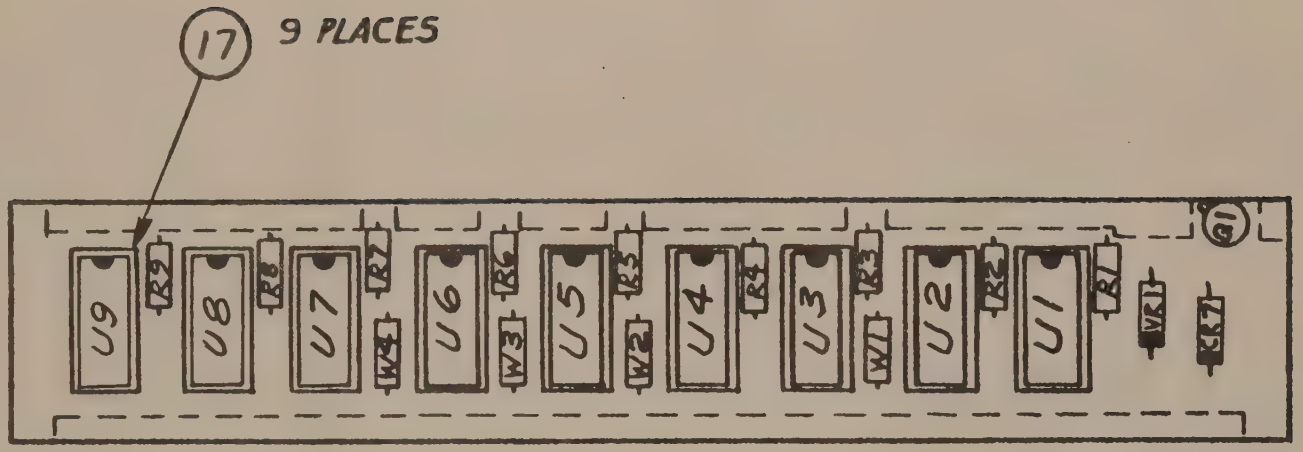
9 DIGIT DISPLAY ASSEMBLY #041945-4-7 REV A_1

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly, Display Board	041766-4-1
	Assembly, Display Driver	041772-4-1
	Schematic	041945-7-2
CR5,6	LED	100455
U7,8,9	Integrated Ckt, DM8880N	045203
V1,2,3	Display Tube, SP352 Sperry	102403
V4	Display Tube, SP353 Sperry	102404
	Spacer LED	101077
	Bracket, Display & Driver	051450
	Driver Assembly DWG.	041772-4-6



NOTE:
1.) ITEMS 36 & 37 TO BE MOUNTED FLUSH TO P.C. BOARD BEFORE SOLDERING.

9 DIGIT DISPLAY BOARD #041766-4-1 REV G_2



NOTE

1) DOTTED AREAS TO BE MASKED BEFORE FLOW SOLDERING.

9 DIGIT DISPLAY DRIVER BOARD #041772-4-6 REV B

PARTS LIST

DISPLAY ASSEMBLY #041766-4-1 REV G_1

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly	041766-4-1
	Schematic	041945-7-2
CR1-4,6	Lamp, LED	100455
R2,4,6	Resistor, 120 Ω ¼w 5%	101717
R7-10	Resistor, 4.7K ¼w 5%	101598
XV1-3	Socket, Display 2 Digit	102445
XV4	Socket, Dispaly 3 Digit	102446
	Spacer, Swage	101062
	Connector, 30 pin Right Angle	101277
	Connector, Mod 6 pin	07189106

PARTS LIST

DISPLAY DRIVER ASSEMBLY #041772-4-1

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly Schematic	041772-4-1 041945-7-2
CR7	Diode, 1N5297	100457
Q1	Transistor, 2N3440	101420
R1-9	Resistor, 10K ¼w 5%	101570
U1-9	Integrated Ckt, DM8880N	045203
VR1	Diode, Zener 180V 1N991B	100461
W1-4	Jumper, Molded	102879
XU1-9	Socket, 16pin	103350

CHAPTER SIX
STANDARD OPTIONS

1) GENERAL

A number of standard options are available for the Model 8132. Standard options, when supplied with the instrument, will be described on the following pages.

CIRCUIT DESCRIPTION
DAYS/ID (OPTION E13)
BLOCK DIAGRAM #7-06103402

1) GENERAL

The Days/ID Option is shown on the instrument Block Diagram. This option adds the #021632-4-21 Days Accumulator Card (A18), Leap Year/ID switch S33, a colon and three-digit display to Display Assembly (A102) and the associated wiring.

Parallel BCD Days/ID outputs are supplied to connector J3 through buffers on the Days Accumulator card. These 12-bits have the following specifications:

Code:	8-4-2-1.
Logic:	"1" = +5 ±0.5 V behind 6 kΩ.
	"0" = 0 +0.5 V, 12 mA sink.

All outputs are short-circuit-proof to ground.

PARTS LIST

DAYS/ID OPTION (E13) #06131615 REV A_2

REF.	DESCRIPTION	SD PART NO.
	ADD	
	Schematic	06103402
A18	Assembly, Days Accumulator	021632-4-21
CR5,6	Lamp, LED	100455
S33	Switch, Slide	102632
U7-9	Integrated Circuit, DD700	045203
V4	Display, SP353	102404
XA18	Connector, P.C.Edge	101204
	Card Guide	021340-1-2
	Eyelet (for S33)	112482
	Spacer, LED	101077
	DELETE	
S33	Cover Plate, Slide Switch	05120802

CIRCUIT DESCRIPTION
DAYS ACCUMULATOR
SCHEMATIC #021632-7-21

1) GENERAL

The Days Accumulator Card can provide up to three serial decades with common reset, parallel preset and two sets of buffered, parallel BCD outputs. Provision is made to gate one set of BCD outputs in three 4-bit bytes. The input may be either AC or DC-coupled and fed to the first decade through an update inhibit circuit. A days recycle circuit is included which may be programmed to reset the accumulator to 001 at the end of 365 or 366 days.

2) DECADE DIVIDERS

The up to three decade dividers are connected in tandem. Each is provided with parallel BCD data inputs which may be used to load preset information when the associated data strobe ($\overline{\text{PRESET}}$) line is grounded. The decade zero-reset inputs are wired in common through buffers on A8 to pin 23. The parallel BCD outputs from each decade are wired to output pins through two sets of buffers.

3) OUTPUT BUFFERS

The BCD output buffers may be inverting or noninverting. One of the two sets (A10, A13 and A15) can be gated by inputs through pins L, K and J, respectively. These gate lines are buffered by inverters A11.

4) INPUT INHIBIT CIRCUIT

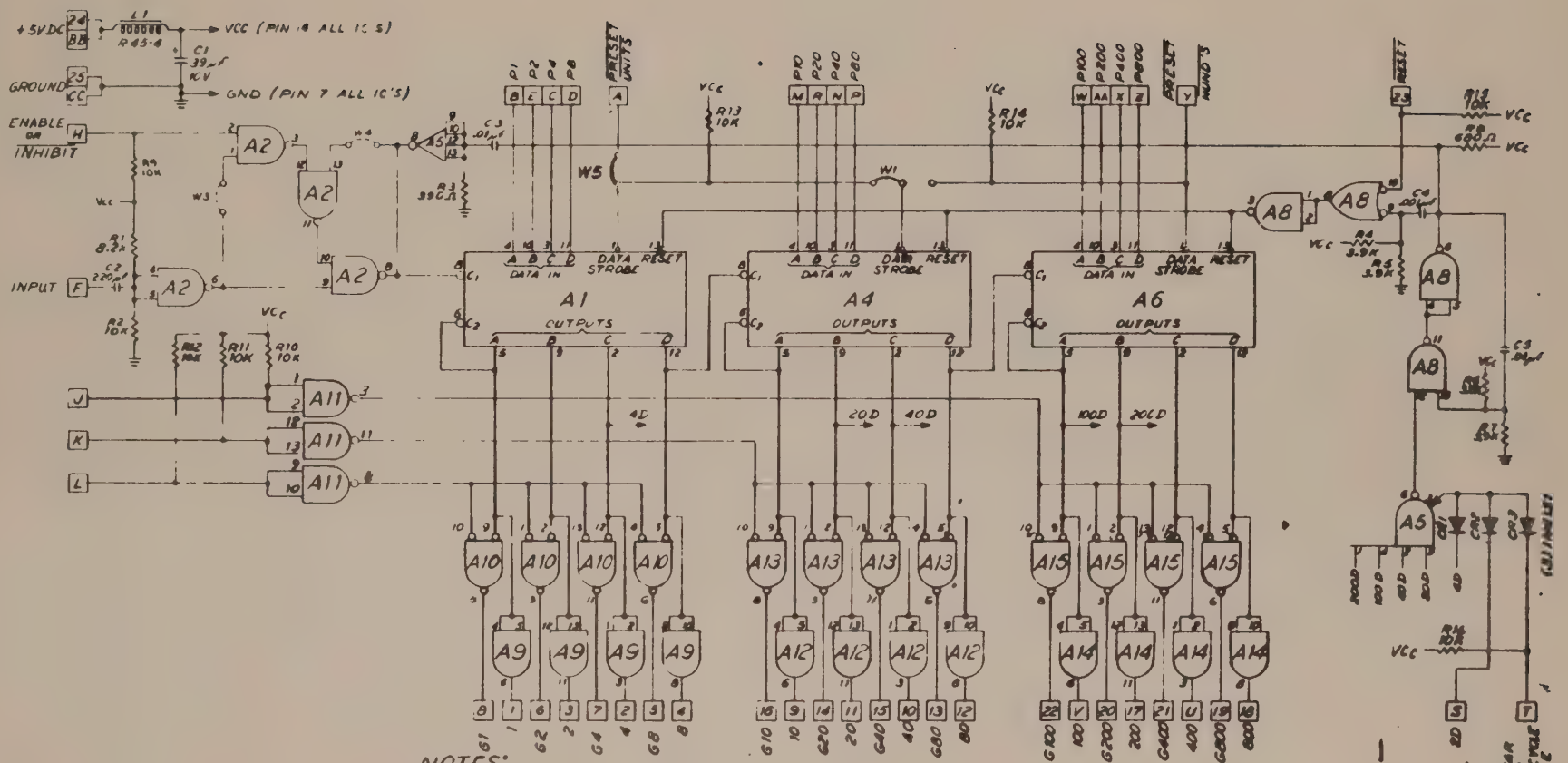
This circuit allows the presence of a ground on pin H to inhibit input signals on pin F from updating the accumulator. Gate A2-6 inverts and buffers the input. Gates A2-11 and A2-8 form an RS flip-flop.

A2-3 gates the $\overline{\text{INHIBIT}}$ line and the inverted input. When the accumulator is updating, flip-flop A2-8,11 output follows the input. When the $\overline{\text{INHIBIT}}$ line, pin H, is grounded, the flip-flop will latch with the output high. The output will go low the first time the input is low after the ground has been removed from the $\overline{\text{INHIBIT}}$ line.

5) DAYS RECYCLE CIRCUIT

Gate 5-6 is a 4-input NAND gate with an expander input. The connection of diodes CR1-CR3 gives the gate seven inputs. If recycle at 366 is desired, pin T is connected to Vcc. If recycle at 367 (for leap year) is desired, pin T is connected to pin 1 (the one day output). Pin S is always connected to the 2-day output. At the selected count, the output of A5-6 will go low, triggering one-shot A8-11,6. The one-shot output is a negative-going pulse (from +5 to 0 V). The leading edge of the pulse (AC-coupled into A8-8) causes the three dividers to reset to 000. The trailing edge of the pulse (which is positive-going) is AC-coupled into A5-8 where it is inverted and used to input one count to the first decade. The resulting accumulator contents are 001.

8132-5-81

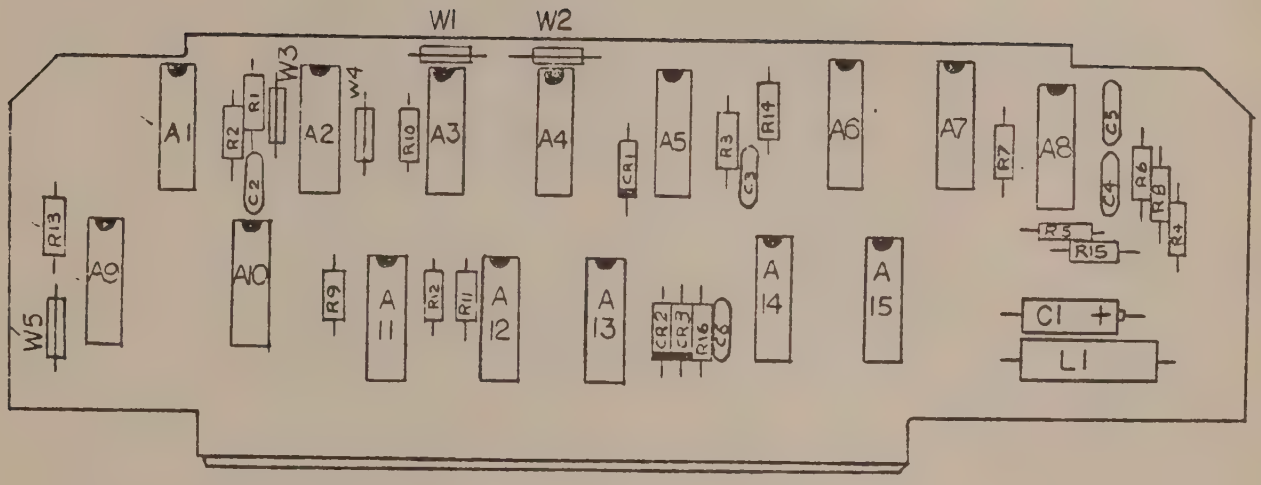


NOTES:

1. INT. CKT. TYPES AS FOLLOWS;
   A1,4,6 = N8280P.
   A2 = MC846P
   A5 - MC830P.
   A8 = SN7400N.
   A9,12,14 = MC1806P.
   A10,13,15 = MC1808P.
   A11 = MC846P.
2. C3 USED FOR DAYS RECYCLE TO "1".
3. FOR TENS TO PRESET WITH UNITS INSTALL W1 AND NOT W2.

DAYS ACCUMULATOR SCHEMATIC #021632-7-21 REV B

OPTION E13-4



DAYS ACCUMULATOR ASSEMBLY #021632-4-1 REV C

PARTS LIST

DAYS ACCUMULATOR #021632-7-21 REV B

REF.	DESCRIPTION	SD PART NO.
	Assembly (Ref. Assy. Dwg. #021632-4-1)	021632-4-21
	Schematic	021632-7-21
A1,4,6	Integrated Circuit, N8280P	025722
A2,11	Integrated Circuit, MC846P	019716
A5	Integrated Circuit, MC830P	019712
A8	Integrated Circuit, SN7400N	019705
A9,12,14	Integrated Circuit, MC1806P	025733
A10,13,15	Integrated Circuit, MC1808P	025734
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 220 pF, Disc	100044
C3,5	Capacitor, .01 µF, Disc	100103
C4	Capacitor, .001 µF, Disc	100076
C6	Capacitor, 100 pF, DM	100173
CR1-3	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
R1	Resistor, 8.2 k, 5%, 1/4 W	101595
R2,9-16	Resistor, 10 k, 5%, 1/4 W	101570
R3	Resistor, 390 Ω, 5%, 1/4 W	101592
R4-7	Resistor, 3.9 k, 5%, 1/4 W	101601
R8	Resistor, 680 Ω, 5%, 1/4 W	101669
W1,5	Jumper, Molded	102879
	Extractor	100865

CIRCUIT DESCRIPTION
BCD MILLISECONDS (OPTION E14)
BLOCK DIAGRAM #7-06103402

1) GENERAL

The BCD Milliseconds Option is shown on the basic unit Block Diagram, Dwg. #7-06103402. This option adds 14-pin rear panel connector J6 and associated wiring.

Parallel BCD Milliseconds outputs are supplied to J6 from buffers on the Minor Counter Card (A9). These 12 bits have the following specifications.

Code:	8-4-2-1.
Logic:	"1" = +5 ±0.5 V behind 6 kΩ.
	"0" = 0 +0.5 V, 12 mA sink.

All outputs are short-circuit-proof to ground.

PARTS LIST

E14 OPTION #06128908 REV A

REF.	DESCRIPTION	SD PART NO.
	ADD	
	Schematic	7-06103402
J6	Connector, 14 Pin, Amph	101180
P6	Connector, 14 Pin, Mating (ship with)	101181
	DELETE	
J6	Connector, Cover Plate, 14 Pin	021398-1-1

CHAPTER SEVEN

SPECIAL MODIFICATIONS

1) GENERAL

Modifications to the Model 8132, requested by the customer, are documented in this chapter. These are usually extra-cost items to tailor the unit for a specific application.

CIRCUIT DESCRIPTION
IEEE 488 BUS INTERFACE WITH COINCIDENCE
FOR MODEL 8132 TIME CODE READER

BLOCK DIAGRAM #7-07160225

1. GENERAL

This feature adds the capability to program and control the Model 8132 Time Code Reader (equipped with Days/ID Option E13 and Coincidence Option A17A) from the IEEE 488 Bus. Provision is included to select Reader Error Bypass and program Coincidence limits from the bus and to provide Status and Time data to the bus. The Coincidence Option circuitry is included as part of the Interface.

2. COINCIDENCE

The Coincidence Option can be programmed and controlled from the front panel when the unit is not under control of the IEEE Bus. It is operational in the Generate and Read Forward Modes of operation. An Enable/Reset switch plus Enable and Alarm indicators are provided on the front panel. The Coincidence limit is entered on the front panel thumbwheel switches.

2.1 MANUAL OPERATION

Operation from the front panel is as follows: The desired Coincidence limit is entered on the thumbwheel switches in days, hours, minutes and seconds. The coincidence circuit is then armed by momentarily moving the ENABLE/RESET switch to the ENABLE position. (The ENABLE indicator should come on.) Coincidence will occur when the time in the Reader Accumulator is equal to the time entered on the switches. At coincidence a pulse is output and a flip-flop is set turning on the ALARM indicator, operating the coincidence relay and outputting the coincidence level signal.

On the trailing edge of the coincidence pulse, the Enable circuit is reset turning off the ENABLE indicator. The flip-flop, ALARM indicator, relay and output level signal remain on, however, until the ENABLE/RESET switch is momentarily moved to the RESET position or an External Reset (ground) pulse is input to the unit. A new limit can now be entered and the circuit can be re-enabled.

CAUTION

When operating from the front panel, the coincidence limit must be set to a time which is greater than the time in the Reader Accumulator or false coincidences can occur.

2.2 SPECIFICATIONS

The coincidence pulse and level output signals, one set of coincidence relay transfer contacts and the external reset input are available on rear panel connector J4.

Coincidence outputs: Positive logic, IC level signals.

Logic "1" = +5 ±0.5 V behind 6 kΩ
Logic "0" = 0 +0.5 V, 12 mA sink.

Relay contacts: 3 A @ 30 V dc or 120 V ac, resistive load. Operate/release time is approximately 20 ms.

External Reset input: A ground true pulse approximately 1 µs in duration.

High = +3 to +5.5 V or open circuit.
(10 kΩ pullup to +5 V provided.)

Low = 0 to +0.5 V, source must sink 1.6 mA.

3. INTERFACE OPERATION

To communicate with the Model 8132, the Bus Controller must place it in the REMOTE Mode of operation by asserting the Remote Enable (REN) line. Then, when the unit is first addressed as a Listener, it will enter the Remote Mode ("REMOTE" indicator on) disabling all front panel Mode controls. The unit will remain in the Remote active Mode until REN goes false or the GTL (Go to Local) message is sent. Device Address is established via rear panel switches S40.

3.1 INTERFACE MESSAGES

The unit is designed to process the following Interface Messages:

3.1.1 UNILINE MESSAGES:

ATN----------Attention
DAC----------Data Accepted
DAV----------Data Valid
IFC----------Interface Clear
REN----------Remote Enable
RFD----------Ready for Data
SRQ----------Service Request

3.1.2 MULTILINE MESSAGES:

GTL----------Go to Local
MLA----------My Listen Address
MTA----------My Talk Address
SPD----------Serial Poll Disable
SPE----------Serial Poll Enable
UNL----------Unlisten
UNT----------Untalk

3.2 DEVICE DEPENDENT COMMUNICATIONS

Device dependent messages are in ASCII characters from the dense subset of the ISO code. They provide for the programming and control of the unit and for the selection and output of Status and Time data. Programming includes the entry of the Coincidence Limit. Control includes Reader Mode selection and Coincidence Enable.

The entry of new instructions automatically overrides previous instructions.

3.2.1 MODE CONTROL

The desired operating mode is programmed by addressing the unit as a Listener and entering the letters "TK" or "TE" defined as follows:

"TK"----------TRANSLATE (READ) with no (KILL) Error Bypass (OE)

"TE"----------TRANSLATE (READ) with Error Bypass (3E)

3.2.2 COINCIDENCE

The Coincidence circuitry can be programmed and enabled from the bus when the unit is operating as a Generator or as a Reader in the forward direction. This is accomplished by addressing the unit as a Listener and entering the following string:

B(n)C

The letter "B" prepares the Time Register to accept the nine digit Coincidence Limit (n) in days, hours, minutes and seconds (most significant digit first). Example: 332 21 49 33.

D H M S

The letter "C" (for Coincidence) arms the Coincidence circuitry and enables generation of a Service Request (see below). The Enable indicator is turned on.

When Coincidence is detected, a Service Request (SRQ) is fed to the bus, the Coincidence pulse and level outputs are generated, the coincidence relay is energized, the Alarm indicator is turned on and the Enable circuit is cleared turning off the Enable indicator. The bus controller identifies the Service Request and can reset the Coincidence circuit by entering the letter "R". The circuit can also be reset by operating the front panel Reset switch or by the External Reset input via J4.

Once reset, the circuit is ready to receive a new Coincidence limit.

3.2.3 SERVICE REQUESTS

Either of two events can initiate a Service Request (SRQ) to the bus. The first of these is Coincidence as described above. When this event occurs, it is identified by Bit 2 being asserted in the response to a Serial Poll.

The second event which can initiate a Service Request is the "EXT STORE" or Freeze command entered via rear panel BNC J14. This signal (a ground pulse) freezes the current time in the Time Data Register on the Time Data Character Serializer Card. Bit 4 is asserted in the response to a Serial Poll.

NOTE

The Time Data Register was in the follow state prior to being frozen. It will return to the follow state after the stored time has been fed to the Bus in response to an Output Time (OT) instruction from the Controller (see below). The Controller responds to the SRQ signal by issuing a Serial Poll Enable (SPE) universal bus message and addressing the unit as a Talker. The unit responds with a Status byte with Bit 2/4 and Bit 7 asserted. The Service Request is cleared by the Serial Poll Disable (SPD) message.

3.2.4 STATUS AND TIME ON DEMAND

Status and Time Data are fed to the Bus as strings of ASCII characters terminated by carriage return (CR) and line feed (LF) characters. Requesting Status or Time does not alter the operation of the unit.

3.2.4.1 STATUS

The Controller requests Status by addressing the unit as a Listener then entering the letter "O" followed by the letter "S" (for Output Status). The letter "O" conditions the unit to interpret the letter "S" as a request for Status. Next, the Controller addresses the unit as a Talker and it feeds a string of sixteen characters to the Bus representing the current status of the unit. This word is defined as follows:

CHARACTER	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	$	SP	|	|	SP		|	SP	|	|	|	SP	SP	CR	LF
READ(TRANSLATE)			T	|			|		|	|	|				
TAPE ERROR				E			|		|	|	|					
REMOTE CONTROL							#		|	|	|					
ERROR BYPASS 0									E	B	0					
ERROR BYPASS 3									E	B	3					

An asterisk (*) is generated when a particular status condition is inoperative, irrelevant or false.

3.2.4.2 TIME

The Controller requests Time by addressing the unit as a Listener then entering the letter "O" followed by the letter "T" as a request for Time rather than as a Read (Translate) command. Next, the controller addresses the unit as a Talker.

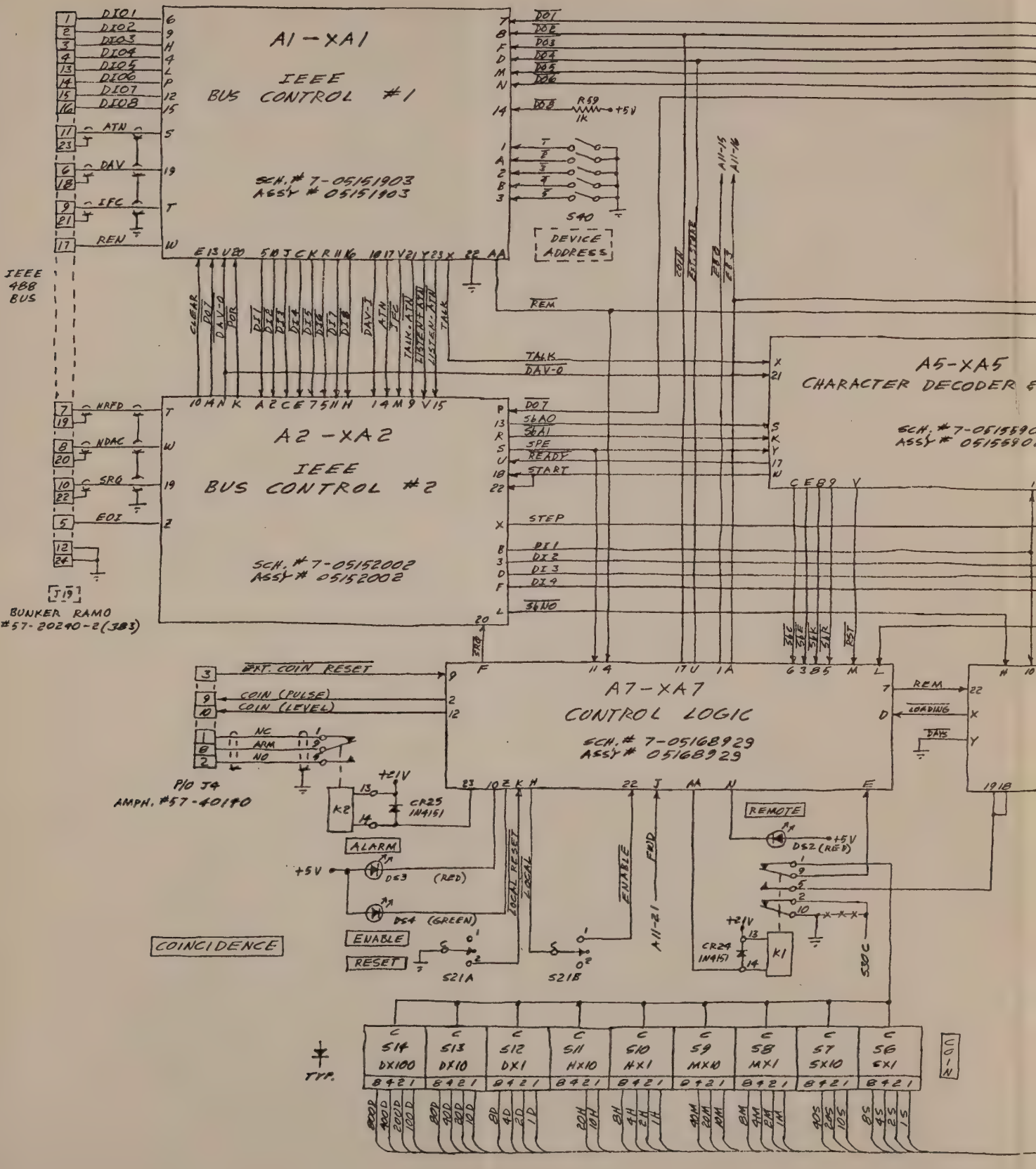
The unit freezes the current time in a register and feeds it to the Bus as a string of fourteen characters as follows: Three digits of days/ID, colon, two digits of hours, colon, two digits of minutes, colon, two digits of seconds, carriage return, line feed.

Example: 365:23:59:59 CR LF

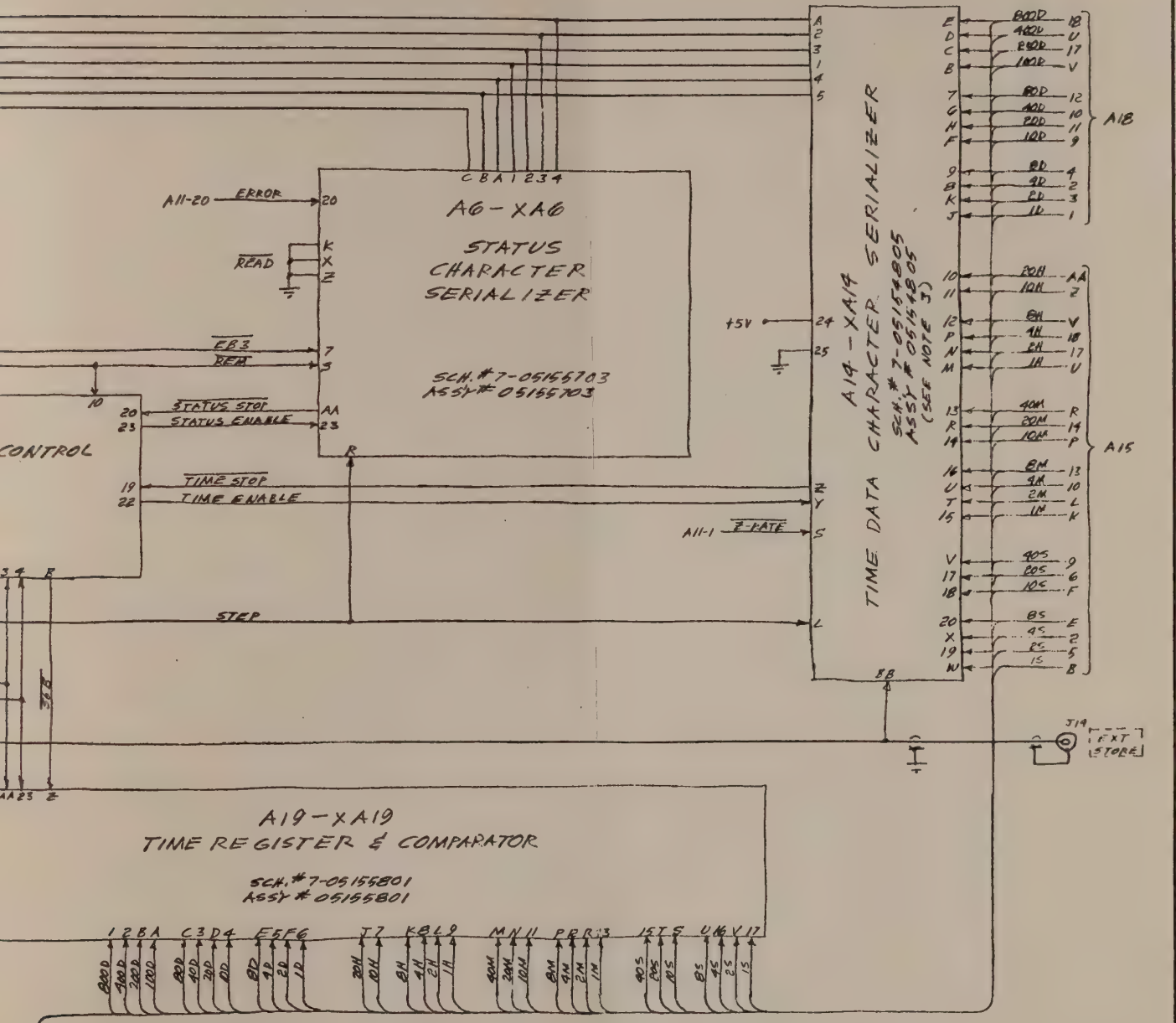
4. CIRCUIT DESCRIPTION

Referring to Block Diagram #7-07160225, the Bus Control Cards (A1 and A2) are shown at the upper left. These cards provide the basic interface to the Bus via J19 mounted on the rear panel. The Device Address switches (S40) are also mounted on the rear panel. The circuitry is enabled when the REM output from A1-AA goes low, operating Remote Control Relay K1 via a driver on A7. Preset Time Data are loaded into registers on Time Register and Comparator Card A19 under control of circuits on A2 and A5.

Character Decoder & Control Card A5 contains an "alpha" decoder armed in the REMOTE Mode of operation. It consists of two 4-16 line decoders, a series of flip-flops and associated gates. The twenty-six letters of the alphabet are decoded and strobed out by signals from A2, A6 and A14. Control Logic Card A7 contains Service Request circuits armed in the REMOTE Mode of operation. Status and Time to the Bus are processed through circuits on Status Character Serializer Card A6 and Time Data Character Serializer Card A14, respectively.


A1 - XA1
IEEE
BUS CONTROL #1
SCH. # 7-05151903
ASSY # 05151903
A2 - XA2
IEEE
BUS CONTROL #2
SCH. # 7-05152002
ASSY # 05152002
A5-XA5
CHARACTER DECODER
A7 - XA7
CONTROL LOGIC
SCH. # 7-05168929
ASSY # 05168929
IEEE 488 BUS
BUNKER RAMO #57-20240-2(383)
P/O J4
AMPH. #57-40140
DEVICE ADDRESS
S40
R59 1K
+5V
EXT. COIN RESET
COIN (PULSE)
COIN (LEVEL)
NC
ARM
NO
+21V
K2
CR25 IN4151
ALARM
D53 (RED)
D54 (GREEN)
ENABLE
RESET
S21A
S21B
LOCAL RESET
LOCAL
REMOTE
D52 (RED)
CR24 IN4151
K1
S20C
COINCIDENCE
TYP.
S14 DX100
S13 DX10
S12 DX1
S11 HX10
S10 HX1
S9 MX10
S8 MX1
S7 SX10
S6 SX1
COIN
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
ATN
DAV
IFC
REN
NRFD
NDAC
SRQ
EOI
CLEAR
DOT
DAV-0
EOR
DAV-I
ATN
IFC
TALK-ATN
LISTEN-ATN
TALK
REM
TALK
DAV-0
DOT
SLAO
SLAI
SPE
READY
START
STEP
DI1
DI2
DI3
DI4
SLNO
SRQ
ENABLE
FUD
A11-21
A11-15
A11-16
LOADING
DAYS

REVISIONS					
REV	DESCRIPTION	ENG. NO.	ECO NO	DATE	APP. BY
A	RELEASED TO RECORD			12/5/81	KAL
A1	J14 PIN 1 WAS 5 & 2 WAS 6.		NFC	9/4/81	RMS



NOTES:

1. THE CIRCUITRY SHOWN IS SUPERIMPOSED ON THE BASIC UNIT EQUIPPED WITH DAYS/ID OPTION E13 (BLOCK DIAGRAM #7-06103402).
2. CARDS, COMPONENTS AND CONNECTORS SHOWN SOLID ARE ADDED. EXISTING COMPONENTS AND CONNECTIONS ARE SHOWN DOTTED. CONNECTIONS SHOWN -X-X-X- ARE DELETED FROM THE BASIC UNIT.
3. GROUND IS CONNECTED TO PINS 25 & CC AND +5V IS CONNECTED TO PINS 24 & BB ON ALL CARDS EXCEPT A14.
4. RELAYS ARE P&B KHP-17D11 24V.

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF NO

LIST OF MATERIALS

PROPRIETARY DATA

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DRAWN	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X .XX .XXX ANGLES ±	SYSTRON DONNER CORPORATION CONCORD, CALIFORNIA
CHECK	DATE		
ENGR	DATE		
MECH	DATE		
PROJ	DATE 8/81		CODE IDENT. 52542
QA	DATE		
SCALE		DO NOT SCALE DRAWING	SH 1 OF 1

IEEE 488 BUS INTERFACE (OPTION FE9D) WITH COINCIDENCE OPTION A17A

USED ON	NEXT ASSY
2132	SN1208
APPLICATION	

MATERIAL

DRAWING NO.

REF	SIZE	PART NO.	REV
7	D	07160225	A.

PARTS LIST
OPTION FE9D (W/A17A) IEEE 488 BUS INTERFACE ASSY. W/COINCIDENCE
#07160225 REV A

REF.	DESCRIPTION	SD PART NO.
	ADD	
	Schematic	7-07160225
A1	Assy., IEEE Bus Control #1 PC	05151903
A2	Assy., IEEE Bus Control #2 PC	05152002
A5	Assy., Character Decoder & Control	05155902
A6	Assy., Status Character Serializer	05155703
A7	Assy., Univ. Logic (Control)	05168929
A14	Assy., Time Data Character Serializer	05154805
A19	Assy., Time Register and Comparator	05155801
CR24,25	Diode, 1N4151	100385
DS2,3	L.E.D., Red	100456
DS4	L.E.D., Green	103202
J14	Connector, BNC	101155
J19	Connector, 24 Cont. (Bunker-Ramo #57-20420-2-383)	117054
	MTG Hardware (For J19)	057361
K1,2	Relay (P&B #KHP-17D11-24V)	101290
R59	Resistor, 1K, 1/4W, 5%	101569
S6,8,10,12, 13,14	Switch Assy., THMBWHL.	05130011
S7,9,11	Switch Assy., THMBWHL. W/Colon	05130012
S21	Switch, Toggle DPDT	102333
S40	Switch, (EECO #240007G)	118705
XA1,2,5,7, 14,19	Connector, P.C. Edge	101204
XK1,2	Relay Socket	102417
XS40	Socket, 14 Pin	118707
	Relay Hold Down Spring	10241701
	Relay Socket Retainer	10241702
	Card Guide	021340-1-2
	Switch End Brkt (PR)	102359
	Switch Strap (PR)	10236709
	Insulator, BNC	100823
	Fiber, Washer	101074
	Ground Lug, BNC	100495

CIRCUIT DESCRIPTION
IEEE BUS CONTROL
SCHEMATICS #7-05151903 AND #7-05152002

1. GENERAL

The basic IEEE Bus Interface is contained on two pc cards: IEEE Bus Control #1 and #2. These cards contain circuitry essential for communications over the bus as required by IEEE Standard 488-1978.

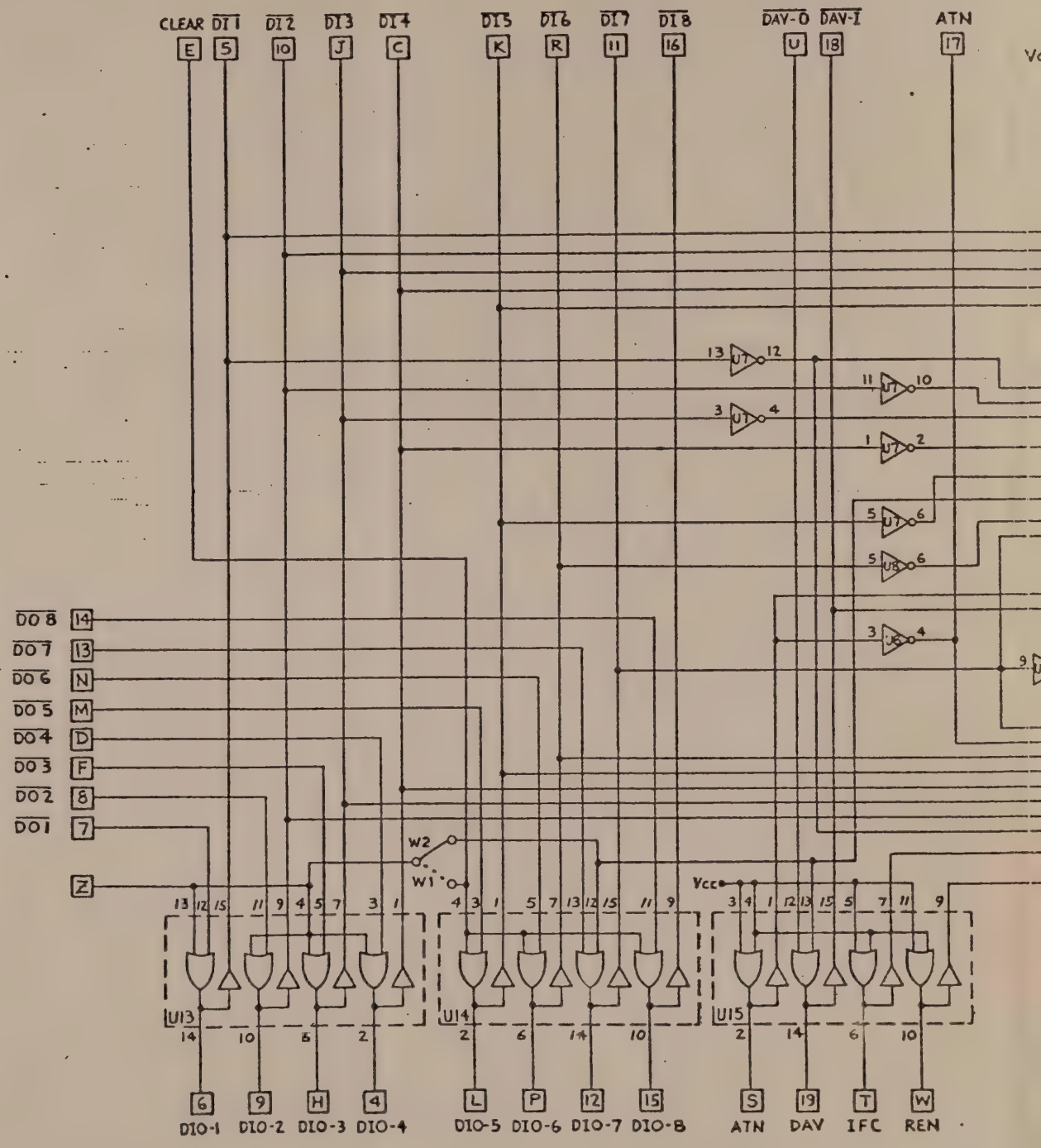
2. CIRCUIT DESCRIPTION

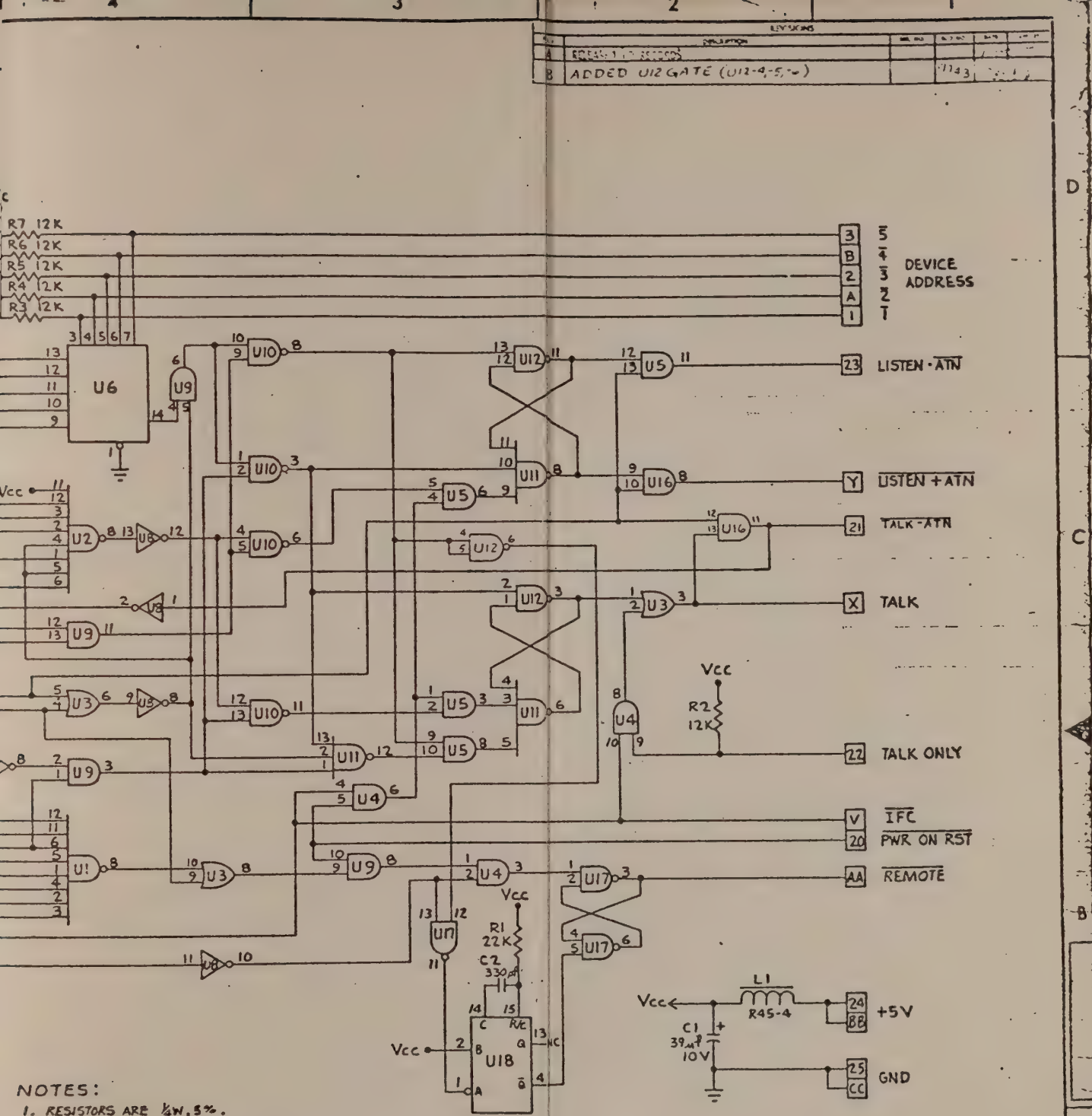
The IEEE Bus Control #1 card contains drivers and receivers on chips U13 through U15 for the eight Data Bus lines (DIO 1-8) plus the Data Valid (DAV), Interface Clear (IFC), Attention (ATN) and Remote Enable (REN) control lines. The drivers are enabled only when the device is designated a Talker. Comparator chip U6 responds when the Device Address selected on external switches appears on the Data Bus. The remaining gates on the card decode and react to the following multiline interface messages: Go To Local (GTL); My Listen Address (MLA); My Talk Address (MTA); Unlisten (UNL) and Untalk (UNT). Flip-flop U12-11/U11-8 or U12-3/U11-6 is set when the device is designated a Listener or a Talker respectively. Each flip-flop is cleared when the other is set. The Talk flip-flop is also cleared if any other device on the bus is designated a Talker. Both flip-flops are cleared by IFC or Power on Reset (pon). Flip-flop U17-6/3 is set (enabling remote control of the device) when the REN line is asserted and the unit is designated a Listener. It is cleared by REN going false or by GTL or pon.

The IEEE Bus Control #2 card contains drivers and receivers on chips U16 and U17 for the Service Request (SRQ); End or Identify (EOI); Not Ready for Data (NRFD) and Not Data Accepted (NDAC) control lines. The NRFD and NDAC drivers are enabled only when ATN is true or when the device is designated a Listener. In these modes the acceptor handshake is provided by one-shots on U12 and flip-flops on U6. One-shot U12-4 provides a delay before assertion of NRFD at U6-6. One-shot U12-5 develops a strobe through gates on U8, U9 and U15 for the loading of data. It sets NDAC flip-flop U6-9 high on the trailing edge provided the READY input to pin U is low.

When the device is designated a Talker the source handshake is provided by one-shots on U5 and U11 plus flip-flops on U10 and U15. Flip-flop U15-6/3 is set by U11-12 output when NRFD is high and the data byte is stable on the Data Bus lines driving the DAV line low through a driver on Control #1 card. It is cleared by U10-8 after a delay through U5-4 when the NDAC line goes high. It is clamped in clear when Talk is cleared. One-shots U5-12 and U11-4, flip-flop U10-5 plus gates U4-3 and U8-8 form a sequencer used to control the loading of data bytes onto the Data Bus.

A Service Request (SRQ) may be initiated by asserting the SRQ line through a driver on U16. Circuitry is included to provide the appropriate response to a Serial Poll from the bus controller. Flip-flop U2-11/8 is set whenever the Serial Poll Enable (SPE) multi-line interface message is detected by decoder U7-8/U1-6. The output from U2-8 drives the DIO-7 Data Bus line low through U4-11, U9-4 and a driver on Control #1 card provided the device is designated a Talker and SRQ is asserted. The U2-11/8 flip-flop is cleared by the Serial Poll Disable (SPD) multi-line message via U7-8/U1-3 or by pon or IFC.


CLEAR
DI1
DI2
DI3
DI4
DI5
DI6
DI7
DI8
DAV-O
DAV-I
ATN
DO8
DO7
DO6
DO5
DO4
DO3
DO2
DO1
W2
W1
Vcc
U13
U14
U15
DIO-1
DIO-2
DIO-3
DIO-4
DIO-5
DIO-6
DIO-7
DIO-8
ATN
DAV
IFC
REN



NOTES:

1. RESISTORS ARE ¼W, 5%.
2. I.C.'s

		GND	Vcc
U1,2	74LS30	7	14
U3	74LS32	7	14
U4,5,9,16	74LS08	7	14
U6	93L24	8	16
U7,8	74LS04	7	14
U10,12,17	74LS00	7	14
U11	74LS10	7	14
U13,14,15	3446	8	16
U18	74LS123	8	16

LIST OF MATERIALS

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF NO

PROPRIETARY DATA

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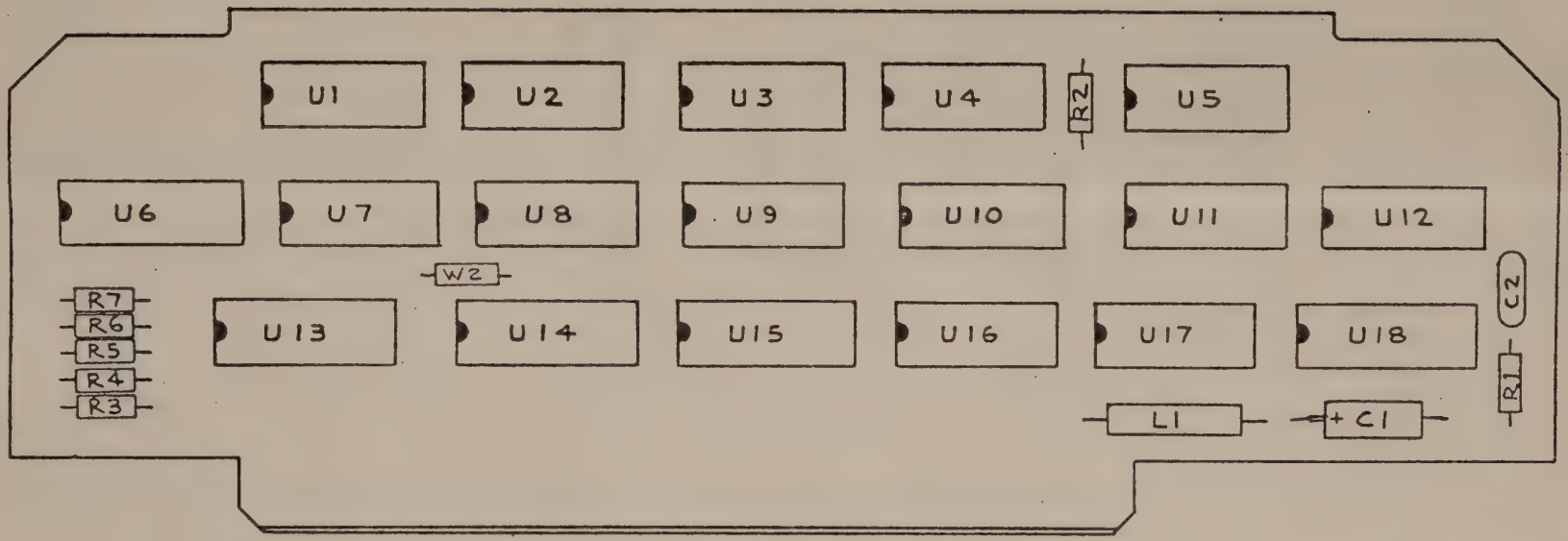
SYSTRON DONNER CORPORATION CONCORD CALIFORNIA		SCHEMATIC, IEEE BUS CONTROL # 1 P.C. BOARD	
CODE IDENT. 52542		DRAWING NO.	
		REV	SIZE	PART NO.
		7	D	051519 03
APPLICATION				



LIST OF MATERIALS

P.C. BD ASSY, IEEE BUS CONTROL № 1

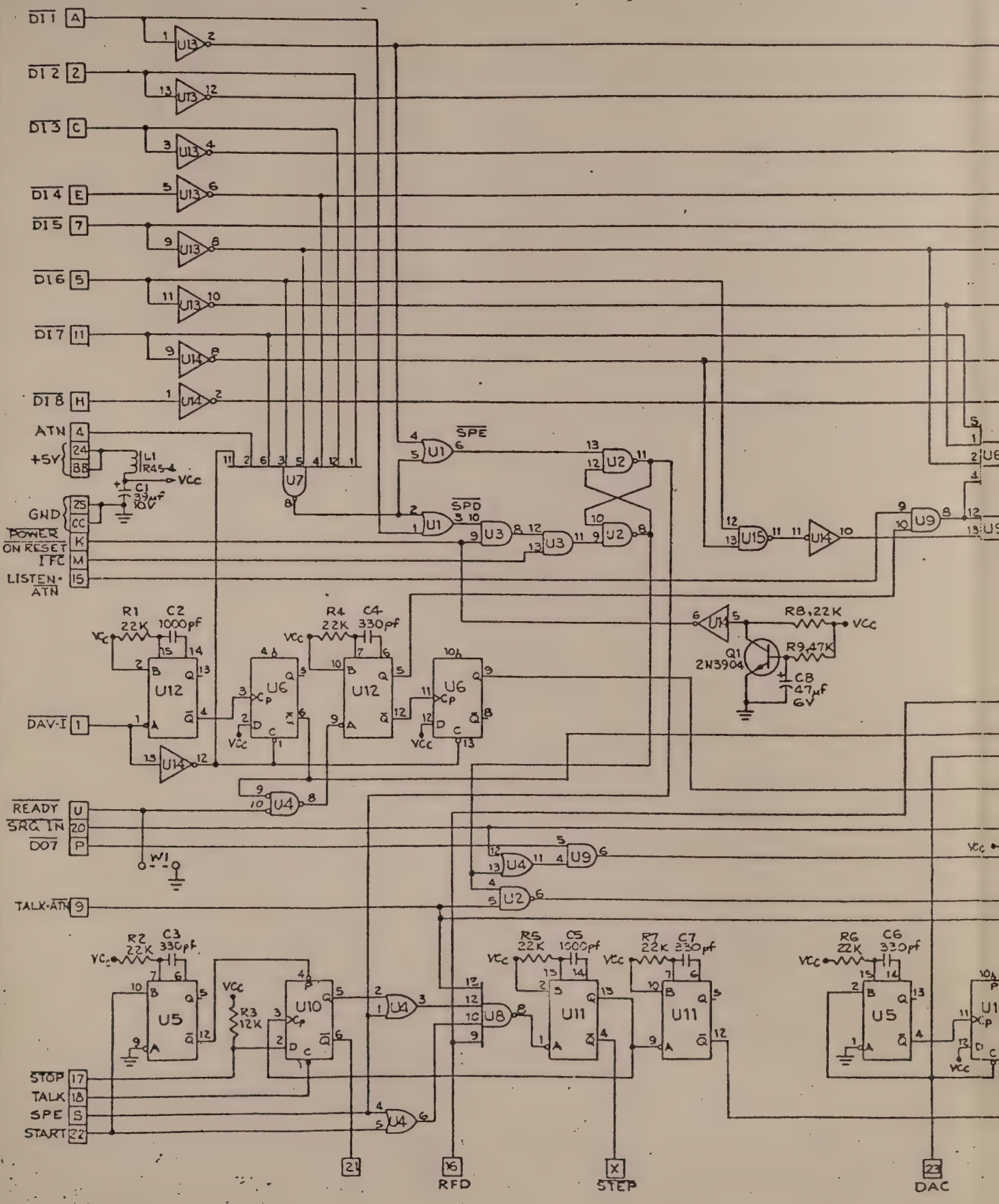
CODE IDENT 57961

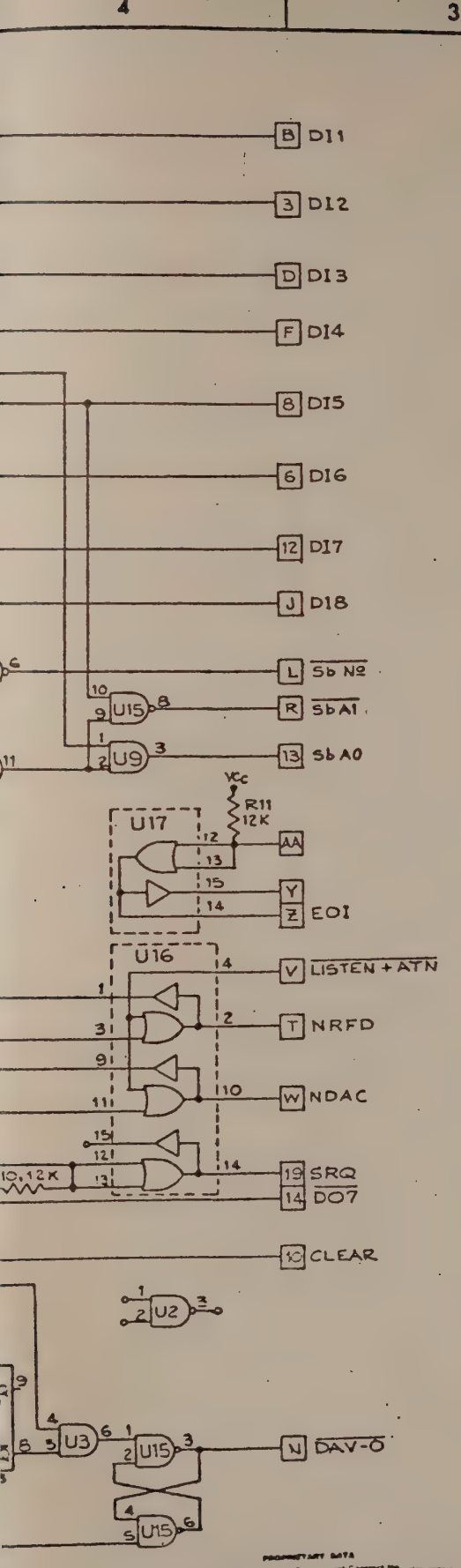
2/1

051590

PARTS LIST
IEEE BUS CONTROL NO. 1
#05151903 REV A

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly	05151903
	Schematic	7-0151903
	Extractor	100865
L1	Inductor, R45-4	101313
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 330 pF, DM	100276
R1	Resistor, 22 K, 1/4 W	101572
R2-7	Resistor, 12 K, 1/4 W	101565
U1	Integrated Circuit, SN74LS30N	103971
U2	Same as U1	
U3	Integrated Circuit, SN74LS32N	103972
U4	Integrated Circuit, SN74LS08N	103967
U5	Same as U4	
U6	Integrated Circuit, 93L24PC	117020
U7	Integrated Circuit	103749
U8	Same as U7	
U9	Same as U4	
U10	Integrated Circuit, SN74LS00N	103130
U11	Integrated Circuit, SN74LS10N	103968
U12	Same as U10	
U13	Integrated Circuit, MC3446	117021
U14	Same as U13	
U15	Same as U13	
U16	Same as U4	
U17	Same as U10	
U18	Integrated Circuit, SN74LS123N	103976
W2	Molded Jumper	102879


DI1 A
DI2 2
DI3 C
DI4 E
DI5 7
DI6 5
DI7 11
DI8 H
ATN 4
+5V 24 BB
GND ZS CC
POWER ON RESET K
IFC M
LISTEN ATN 15
DAV-I 1
READY U
SRQ IN 20
DO7 P
TALK-ATN 9
STOP 17
TALK 18
SPE S
START 22
21
16 RFD
X STEP
23 DAC
VCC
GND
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
SPE
SPD
L1 R4S-4
C1 39µf 10V
R1 22K
C2 1000pf
R2 22K
C3 330pf
R3 12K
R4 22K
C4 330pf
R5 22K
C5 1000pf
R6 22K
C6 330pf
R7 22K
C7 330pf
R8 22K
R9 47K
Q1 2N3904
C8 47µf 6V
W1



NOTES

1. RESISTORS ARE ¼W, 5%.
2. I.C.'s

SCH REF	TYPE	GND	VCC
U1,4	74LS32	7	14
U2,15	74LS00		
U3,9	74LS08		
U5,11,12	74LS123	8	16
U6,10	74LS74	7	14
U7	74LS30		
U8	74LS20		
U13,14	74LS04		
U16,17	3446	8	16

REVISIONS

REV	DESCRIPTION
A	

LIST OF MATERIALS

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMAL TOLERANCE
.X ±
.XX ±
.XXX ±
ANGLES ±

DRAWN DATE
CHECK DATE
ENGR DATE
PROJECT DATE
QA DATE
SCALE DO NOT SCALE DRAWING
SHEET 1 OF 1
MATERIAL

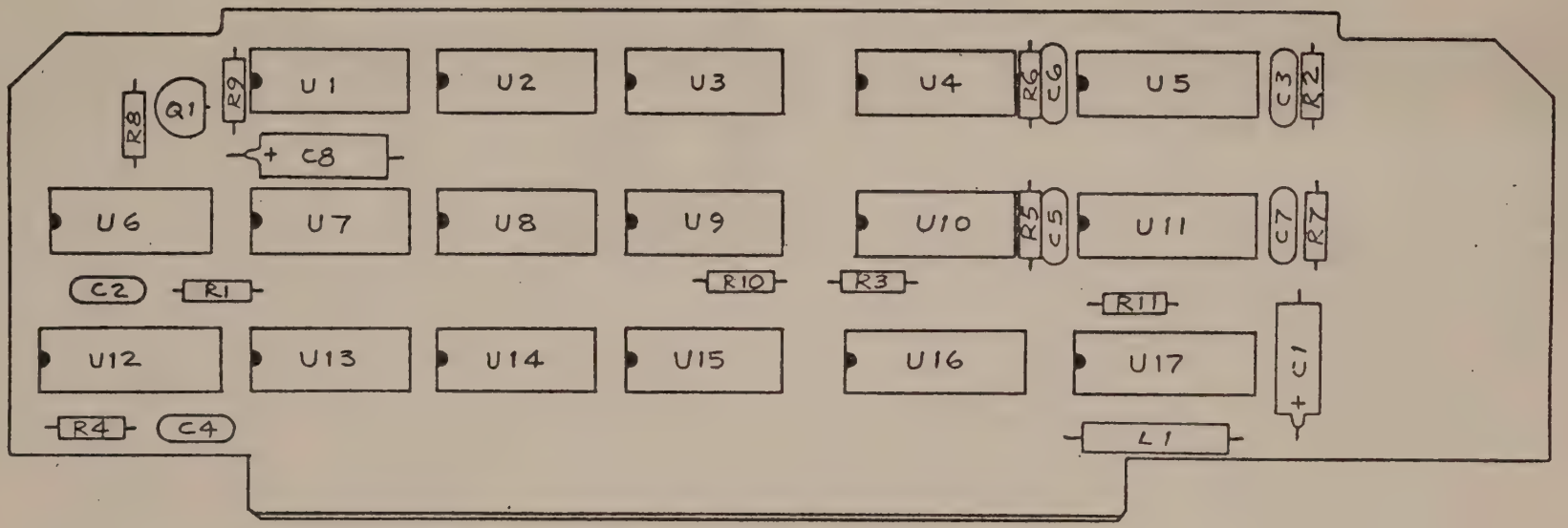
SYSTRON DONNER CORPORATION
CONCORD CALIFORNIA
CODE IDENT. 52542

IEEE BUS CONTROL #2

DRAWING NO
REV | SIZE | PART NO | REV
7 | D | 05152002 | A

FIELD CH | NEXT ASSY
APPLICATION

PROPRIETARY DATA



LIST OF MATERIALS

DYSTRON DONNER CORPORATION CONCORD CALIFORNIA

CODE IDENT 52542

P.C. ASSY., IEEE BUS CONTROL Nº 2

B 05152002 A

PARTS LIST
IEEE BUS CONTROL NO. 2
#05152002 REV B

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly	05152002
	Schematic	7-05152002
	Extractor	100865
L1	Inductor, R45-4	101313
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 1000 pF, DM	100243
C3-C7	Capacitor, 330 pF, DM	100276
C8	Capacitor, 47 µF, 6V Tant	100224
Q1	Transistor, 2N3904	101377
R1	Resistor, 22 K 1/4 W	101572
R2	Same as R1	
R3	Resistor, 12 K 1/4 W	101565
R4	Same as R1	
R5	Same as R1	
R6	Same as R1	
R7	Same as R1	
R8	Same as R1	
R9	Resistor, 47 K 1/4 W	101574
R10	Same as R3	
R11	Same as R3	
U1	Integrated Circuit, SN74LS32N	103972
U2	Integrated Circuit, SN74LS00N	103130
U3	Integrated Circuit, SN74LS08N	103967
U4	Same as U1	
U5	Integrated Circuit, SN74LS123N	103976
U6	Integrated Circuit, SN74LS74N	103132
U7	Integrated Circuit, SN74LS30N	103971
U8	Integrated Circuit, SN74LS20N	103969
U9	Same as U3	
U10	Same as U6	
U11	Same as U5	
U12	Same as U5	
U13	Integrated Circuit, SN74LS04N	103749
U14	Same as U13	
U15	Same as U2	
U16	Integrated Circuit, MC3446P	117021
U17	Same as U16	

CIRCUIT DESCRIPTION
CHARACTER DECODER AND CONTROL
SCHEMATIC #7-05155902

1. GENERAL

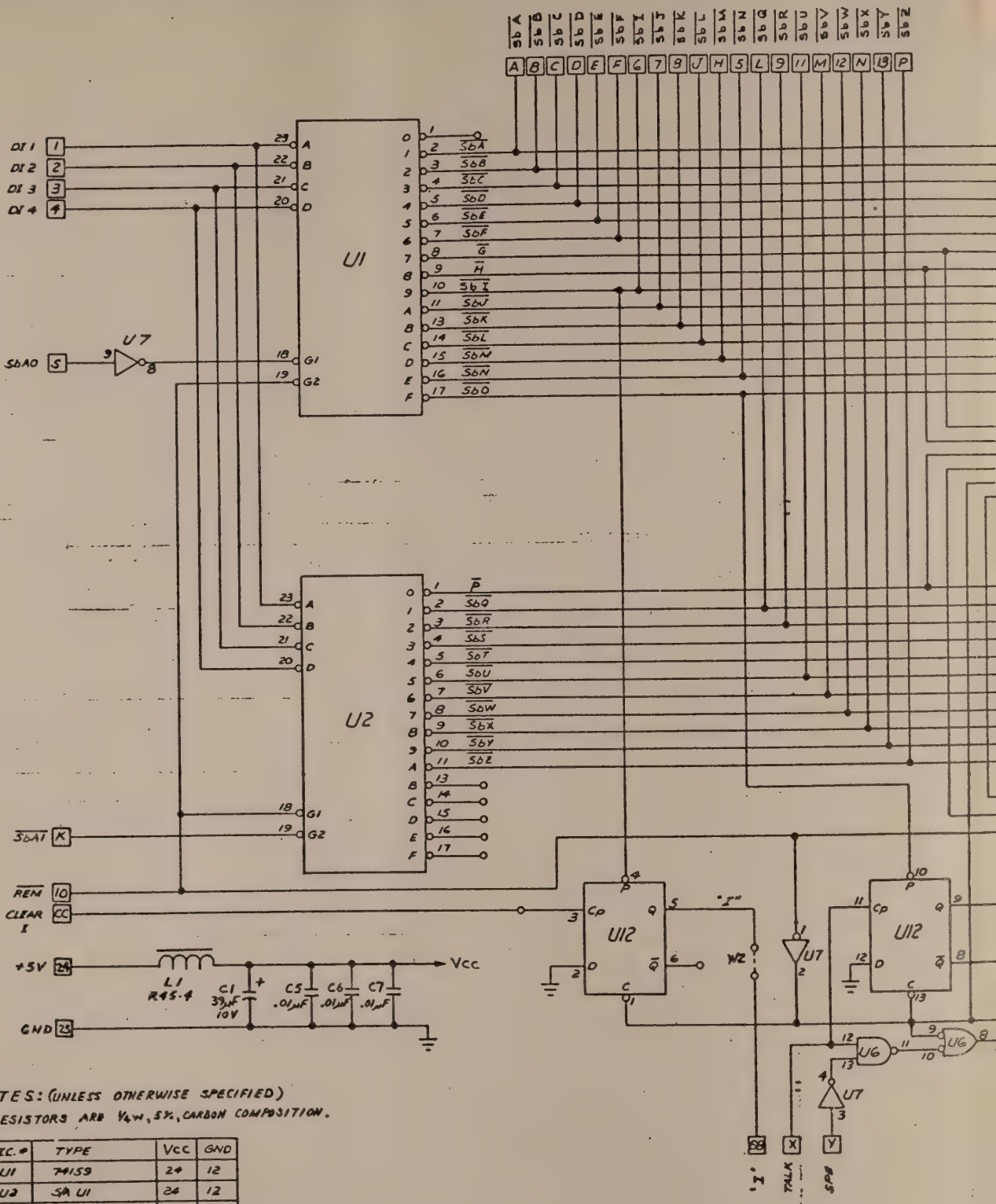
This card accepts the first four Data bits and the associated "Alpha" strobes from the IEEE Bus Control and decodes all characters in columns 4 and 5 of the ISO Code. In addition, it includes a four-state flip-flop for Generator Mode storage and circuits for Input/Output steering and Time/Status enable.

2. CIRCUIT DESCRIPTION

Referring to the Schematic, the character decoders (U1 and U2) are shown at the left. These decode all 32 characters in columns 4 and 5 of the ISO Code. Of these, the 26 letters of the alphabet are selected. Of the 26 letters, 22 are provided as strobed outputs from the card, 3 (G, H and P) are stored in the four-state flip-flop (formed from gates on U3 and U5) and 1 (O) is stored in Output flip-flop U12-9.

The four-state flip-flop stores the selected Generator mode of operation. The Output flip-flop steers SbT and SbS signals to the Time and Status Enable flip-flops (on U11), respectively, when the output of Time or Status to the IEEE Bus is requested.

Timer U13 is used to release the bus after one second in the event that preset of the Generator is unsuccessful.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE ¼W, 5%, CARBON COMPOSITION.

2.

IC.#	TYPE	Vcc	GND
U1	74LS9	24	12
U2	S/A U1	24	12
U3	74LS22	14	7
U4	1808	14	7
U5	S/A U3	14	7
U6	74LS00	14	7
U7	74LS04	14	7
U8	16 PIN RES. MOD USX	16	—
U9	S/A U8	16	—
U10	1806	14	7
U11	74LS74	14	7
U12	S/A U11	14	7
U13	555	8	1

REVISIONS					
REV	DESCRIPTION	MFR. NO.	ECO NO	DATE	APP BY
A	RELEASE TO RECORDS			7-29	BH

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

PROPRIETARY DATA

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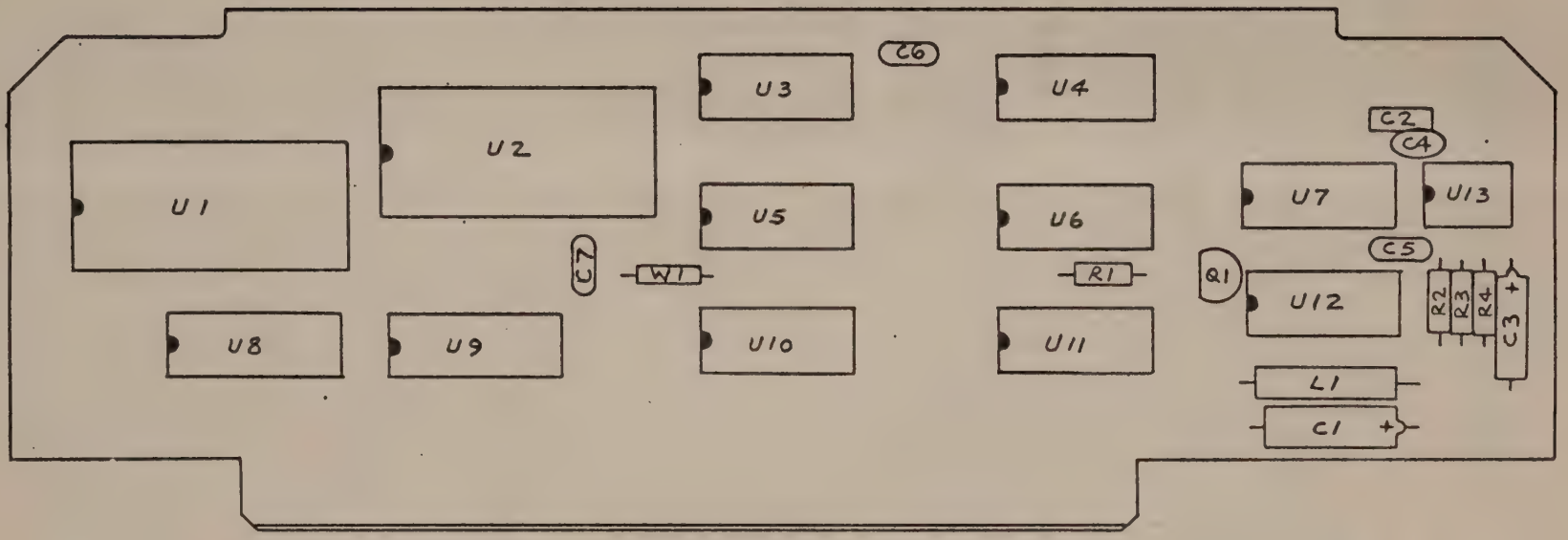
DRAWN 8/1/71 DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±.01 .XX ±.005 .XXX ±.002 ANGLES ±	SYSTRON DONNER CORPORATION CONCORD, CALIFORNIA
CHECK DATE		
ELECT. DATE		
MECH. DATE		
PROJ. DATE		
QA DATE		
8100		CODE IDENT. 52542
USED ON / NEXT ASSY	SCALE ~	MATERIAL
APPLICATION	DO NOT SCALE DRAWING	SH 1 OF 1

SCHEMATIC: CHARACTER DECODER & CONTROL PC. BD

DRAWING NO.			
REF	SIZE	PART NO.	REV
7	D	05155902	A

REV	DESCRIPTION	DATE	APPROVED
A	RELEASED TO RECORDS		



LIST OF MATERIALS

		CONTRACT NO.	P.C. ASSY., CHARACTER DECODER & CONTROL
		CONCORD CALIFORNIA	
		CODE IDENT 52342	
8100		SCALE 2:1	SIZE B, PART NO 05153902, REV A

PARTS LIST
CHARACTER DECODER & CONTROL #05155902 REV A

REF.	DESCRIPTION	SD PART NO.
	Assembly	05155902
	Schematic	7-05155902
C1	Capacitor, 39 F, 10 V	100183
C2	Capacitor, .001 F	100251
C3	Capacitor, 1 F, 10 V, TANT.	100082
C4,5,6,7	Capacitor, .01 F, Cer. Dp.	117570
L1	Inductor, R45-4	101313
Q1	Transistor, 2N3904	101377
R1	Resistor, 390 , 1/4 W, 5%	10159201
R2	Resistor, 10 k, 1/4 W, 5%	10157001
R3	Resistor, 8.2 k, 1/4 W, 5%	10159501
R4	Resistor, 820 k, 1/4 W, 5%	10185001
U1,2	Integrated Ckt., 74159	
U3,5	Integrated Ckt., 74LS22	116914
U4	Integrated Ckt., 1808	025734
U6	Integrated Ckt., 74LS00	103130
U7	Integrated Ckt., 74LS04	103749
U8,9	Integrated Ckt., 15 k Res. Module	102925
U10	Integrated Ckt., 1806	025733
U11,12	Integrated Ckt., 74LS74	103132
U13	Integrated Ckt., 555	045208
W1	Jumper, Molded	
	Extractor	100865

CIRCUIT DESCRIPTION
MILLISECONDS AND STATUS CHARACTER SERIALIZER
SCH. #7-05155703

1. GENERAL

This card accepts and stores BCD Milliseconds time data which it outputs character serial, bit parallel (under control of signals from the Time Data Character Serializer Card, Schematic #7-05154805) when milliseconds are included in the interface.

It accepts system status signals which are encoded in ASCII and output character serial under control of external enable and step inputs. The status format is shown at the lower left on Schematic #7-05155703.

2. CIRCUIT DESCRIPTION

Referring to the Schematic, millisecongds time data from Minor Counter are loaded into the register formed from U11 through U13 by a Sb Time signal which occurs each millisecond during normal operation. This signal is input from the Time Data Character Serializer (Schematic #7-05154805) along with character select signals E, F and 10. Data are output through tri-state drivers on U10. A mask output (pin 22)is generated when milliseconds are selected .

When status data are to be output, the status enable input to pin 23 goes high and stays high during the entire sequence. This signal enables decoder U8, counter U7 and the first tri-state outputs on PROM U9. The first step input to pin R selects the first character ($) for output. This is followed by a space character (SP). The next character (#3) indicates the Reader/Generator Mode as follows:

STOP(PRESET)----------"P"
HOLD----------"H"
GENERATE----------"G"
Translate(READ)----------"T"

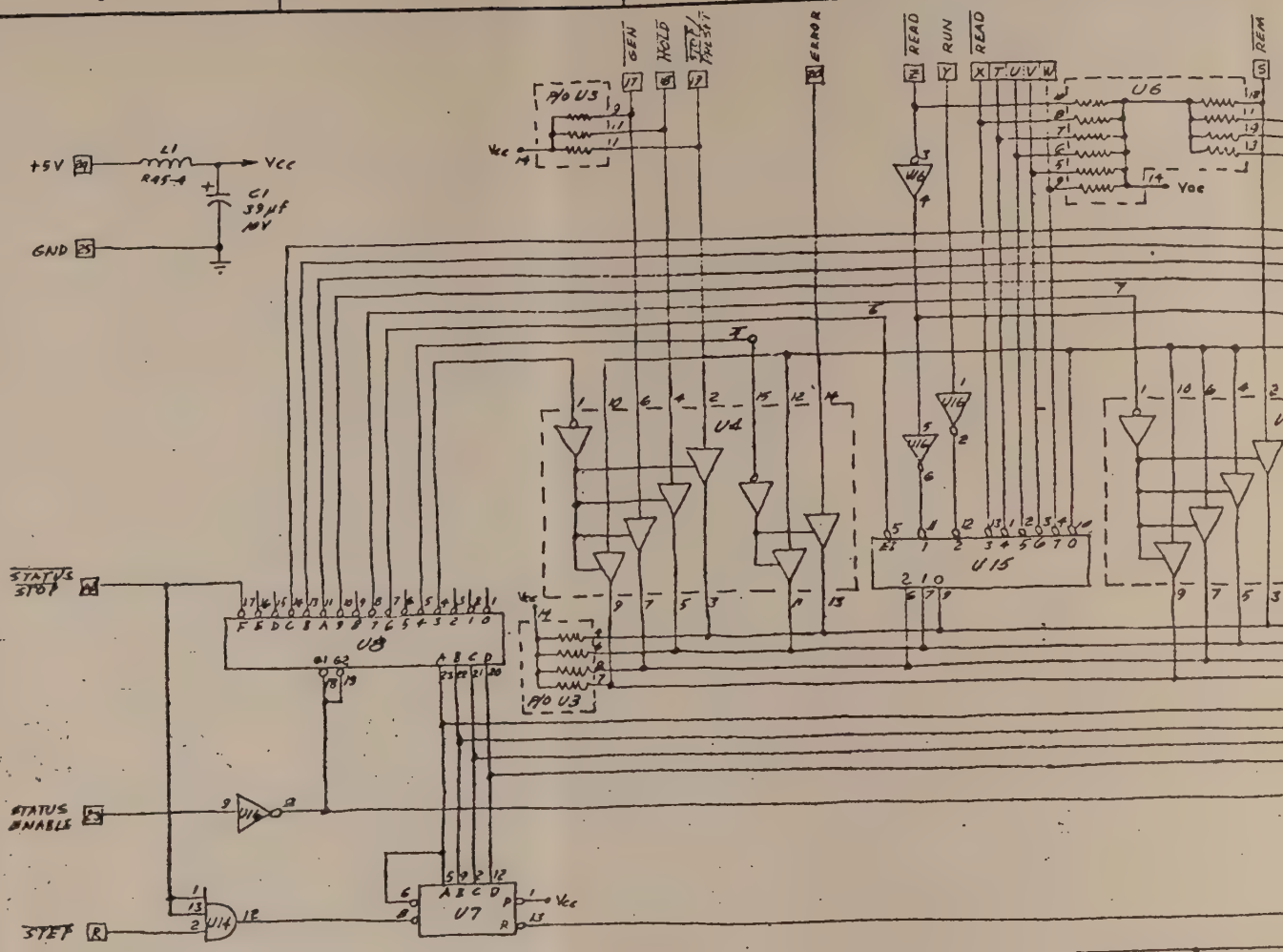
The next character (#4) indicates a possible tape error if the unit is in READ Mode. The letter "E" is output if an error was detected. Otherwise an asterisk (*) character is output. This is followed by a space (SP) character.

The next character (#6) indicates that the Generator is running (R). Character #7 indicates if the unit is under remote control or local (front panel) control. The pound symbol (#) is output if the unit is in REMOTE.

NOTE: When used with IEEE Bus Interface, this character is redundent since the Controller must place the unit in REMOTE before it can get status.

This is followed by a space (SP) character. The next three characters(#9, A and B) indicate if the unit is in Error Bypass Mode(EB3) or if the Error Bypass Mode is discarded (EBO).

The remaining characters (D,E &F) consist of a space (SP) followed by a carriage return (CR) and line feed (LF). The status characters are stored in Prom U9. They are addressed by Counter U7 and selected from encoder U15 and tri-state drivers on U1, U2 ,U4 and U5. These are enabled by the outputs from decoder U8.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. IC's

		Vcc	GND
U1,2,4,5	74LS367	16	8
U3,6	(13) 10K RES PACK	14	—
U7	74LS197	14	7
U8	74154	24	12
U9 (MMI 6308-1)	0813 0603	20	10
U10	SN74LS366N	16	8
U11,12,13	SN74LS173N	16	8
U14	74LS11	14	8
U15	SN74LS30BN	16	8
U16	74LS04	14	7

2. STATUS FORMAT;

CHARACTER 1 2 3 4 5 6 7 8 9 A B C D E F

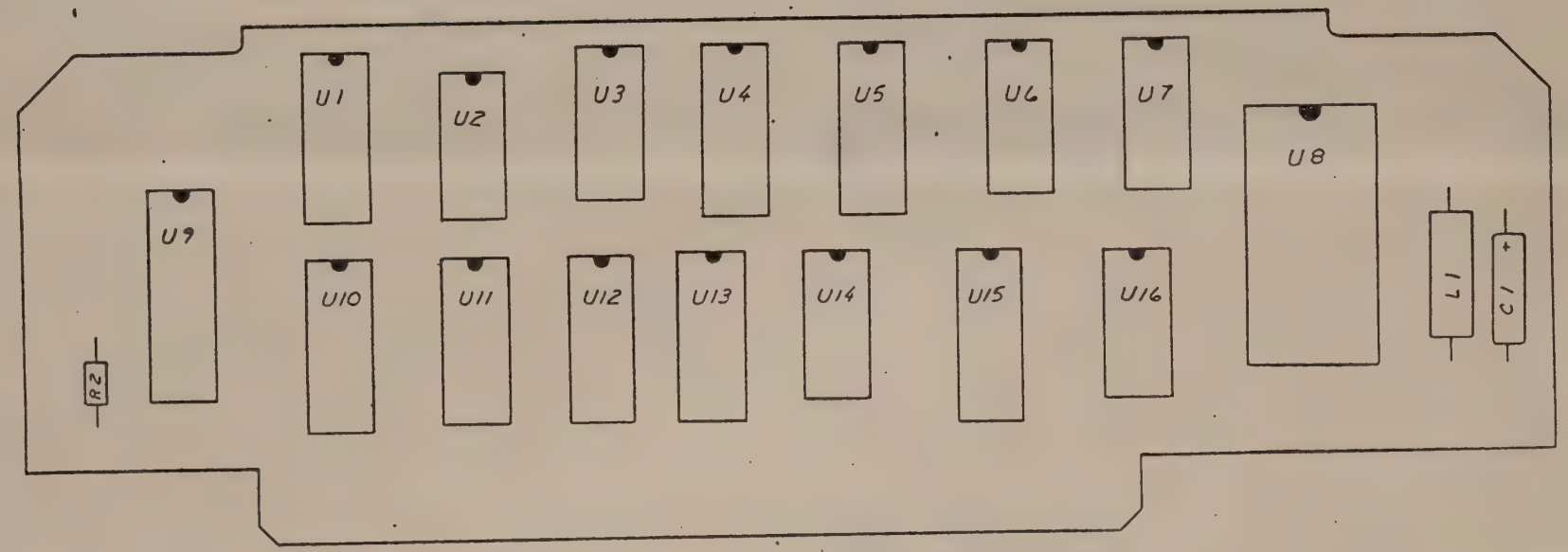
		#	SP		SP		SP						SP	SP	CR/LF
R/C MODE	SEND/RECEIVE		P												
	HOLD		H												
	GENERATE		G												
	READ (TRANS)		T												
TAPE ERROR			E												
GEN. RUNNING					R										
REMOTE CONTROL							#								
ERROR BYPASS 0										E	B	0			
ERROR BYPASS 3										E	B	3			

3. U9 PROGRAMMING (NEGATIVE LOGIC);

ADD.	CH.	$b_7 b_6 b_5 b_4 b_3 b_2 b_1$	ADD.	CH.	$b_7 b_6 b_5 b_4 b_3 b_2 b_1$
1F	$	0 1 0 0 1 0 0	BF	SP	0 1 0 0 0 0 0
2F	SP	0 1 0 0 0 0 0	93	*	0 1 0 1 0 1 0
33	G	1 0 0 0 1 1 1	97	E	1 0 0 0 1 0 1
35	H	1 0 0 1 0 0 0	AE	B	1 0 0 0 0 1 0
36	P	1 0 1 0 0 0 0	AF	*	0 1 0 1 0 1 0
37	T	1 0 1 0 1 0 0	BC	*	0 1 0 1 0 1 0
4C	*	0 1 0 1 0 1 0	BD	*	0 1 0 1 0 1 0
4D	E	1 0 0 0 1 0 1	BE	3	0 1 1 0 0 1 1
5F	SP	0 1 0 0 0 0 0	BF	0	0 1 1 0 0 0 0
6C	*	0 1 0 1 0 1 0	C7	SP	0 1 0 0 0 0 0
6D	R	1 0 1 0 0 1 0	CF	SP	0 1 0 0 0 0 0
6F	*	0 1 0 1 0 1 0	DF	SP	0 1 0 0 0 0 0
70	#	0 1 0 0 0 1 1	EF	CR	0 0 0 1 1 0 1
71	*	0 1 0 1 0 1 0	FF	LF	0 0 0 1 0 1 0

4. AN ASTERISK (*) IS GENERATED WHEN A PARTICULAR STATUS CONDITION IS INOPERATIVE, IRRELEVANT OR FALSE.

REVISIONS
REV
DESCRIPTION
A
RELEASED TO RECORDS
STATUS CHARACTER GENERATOR
READ
P/O U3
U1
U2
U9
U10
U11
U12
U14
R2
10K
1/4W, 5%
MILLISECONDS
REF: DWG # 7-051548 05 FOR DESCRIPTION OF TIME FORMAT.
DO7
DO6
DO5
DO4
DO3
DO2
DO1
MASK
PROPRIETARY DATA
LIST OF MATERIALS
ITEM NO
QTY
PART NUMBER
DESCRIPTION
SCHEMATIC REF NO
SYSTRON DONNER
CORPORATION
CONCORD CALIFORNIA
CODE IDENT 52542
MILLISECONDS AND STATUS CHARACTER SERIALIZER
DRAWING NO
REF
SIZE
PART NO.
7
D
251557 03
APPLICATION
USED ON
NEXT ASSY
SCALE
DO NOT SCALE DRAWING
SHT 1 OF 1



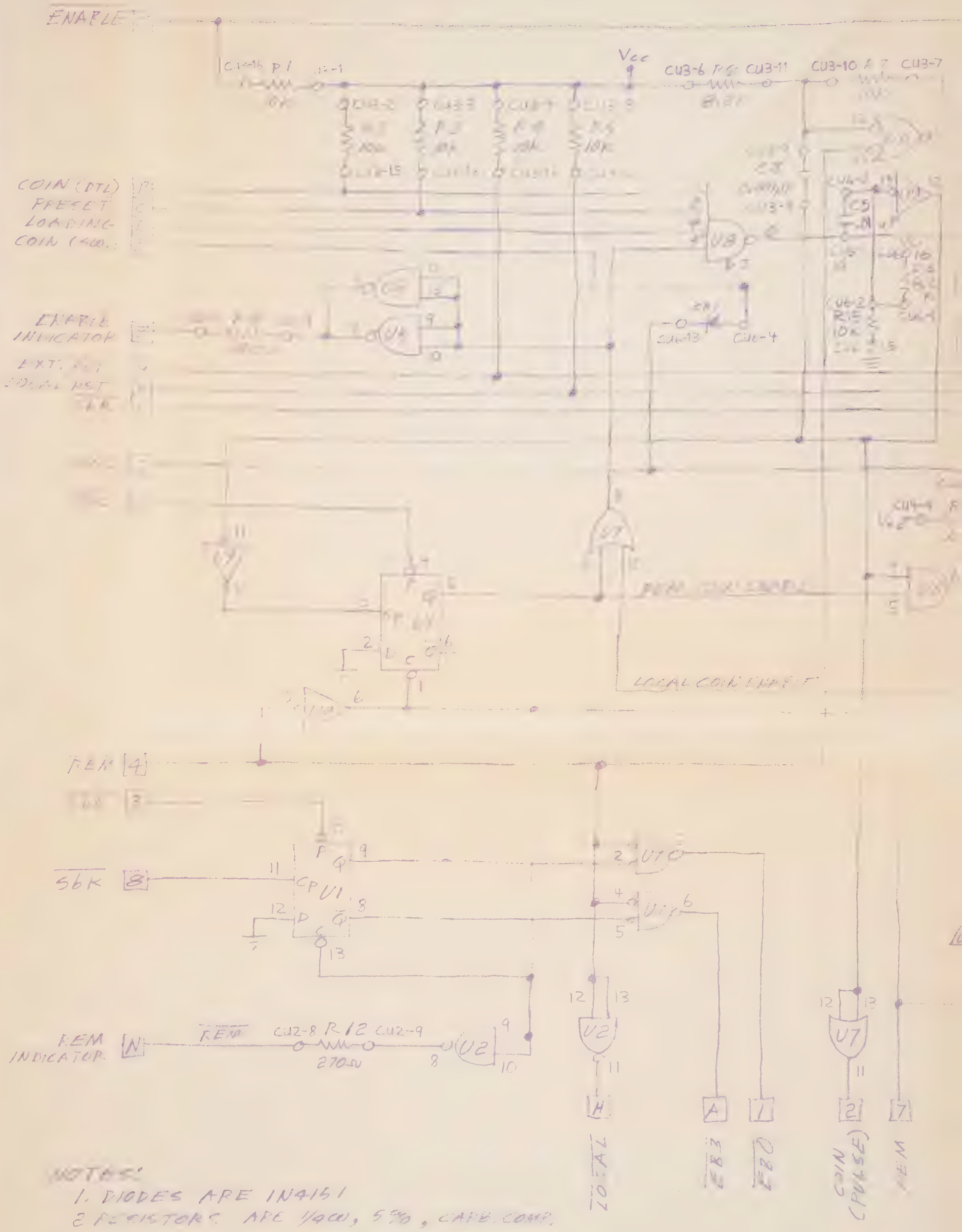
LIST OF MATERIALS

STATUS SERIALIZER

CODE IDENT 52542

PARTS LIST
MS & STATUS CHARACTER SERIALIZER #05155703 REV A

REF.	DESCRIPTION	SD PART NO.
	Assembly	05155703
	Schematic	7-05155703
C1	Capacitor, 39 µF	100183
L1	Inductor, R45-4	101313
R2	Resistor, 10 k, 1/4 W	10157001
U1,2,4,5	Integrated Ckt., 74LS367	116429
U3,6	Integrated Ckt., 10 k Res Pk, Beckman	117241
U7	Integrated Ckt., 74LS197	103165
U8	Integrated Ckt., 74154	106640
U9	Integrated Ckt., Programmed Prom	08130603
	Integrated Ckt., Prom (MMI 6308-1)	117849
U10	Integrated Ckt., SN74LS366AN	118702
U11,12,13	Integrated Ckt., SN74LS173N	118699
U14	Integrated Ckt., 74LS11	116323
U15	Integrated Ckt., SN74LS348N	118700
U16	Integrated Ckt., 74LS04	103749
	Extractor	100865



NOTES:

1. DIODES ARE IN4151
2. RESISTORS ARE 1/4W, 5%, CARB. COMP.
3. IC's

U1, U4	74LS74
U2	846
U5	7400
U7, U10	1508
U8	830
U9	7409
U11	7408

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REVISIONS					
REV.	DESCRIPTION	ENG. NO.	ECO NO.	DATE	APP. BY
A					
A1					

D

C

B

A

CU12-7 COIN — E3 COIN

CU12-6 — Q1 2N2222 — CU12-5

C19-9 P11 C19-8 — CU4-4 — V0 COIN ALARM INDICATOR

210Ω

CR2 CR3 CU6-10 P10 CU6-7 — VCC

CU6-5 CU6-6 CU6-11

10K

CU4-8

CU6-9 — C4 — C16-8

CU4

F SR4

CU12-15 R13 CU12-2 — CU12-2 — Q2 — CU12-3 — PEM RLY DRIVE

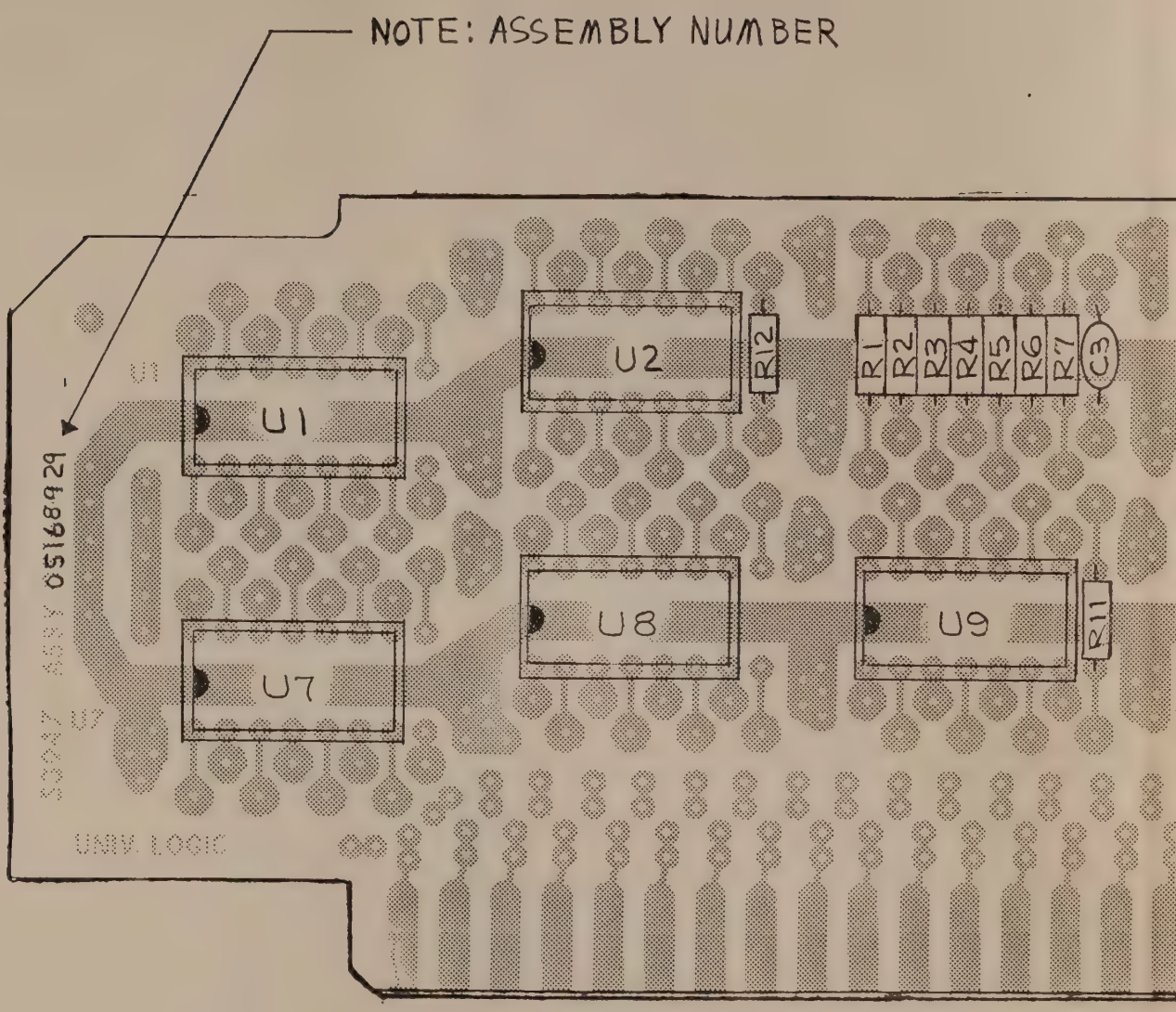
330Ω

CU12-1

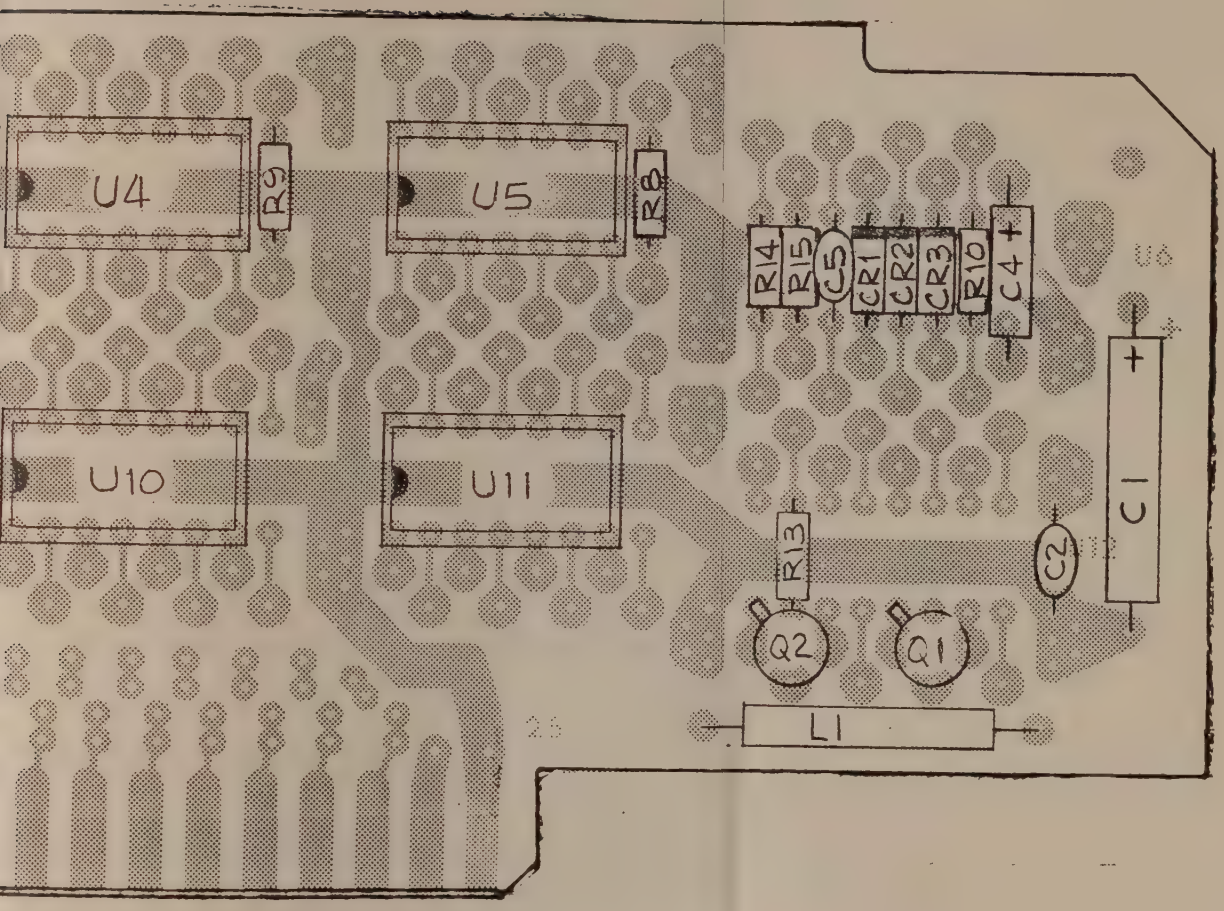
ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

BIZE	S/N 1208	DRAWN DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	SYSTRON DONNER CORPORATION CONCORD, CALIFORNIA
214 2	4/11/74	CHECK DATE	DECIMAL TOLERANCE	CONTROL LOGIC
USED ON	NEXT ASSY	ELECT DATE	.X	CODE IDENT. 52542
APPLICATION		MECH. DATE	.XX	
		PROJECT DATE	.XXX	DRAWING NO.
		QA DATE	ANGLES ±	REF 7 SIZE C PART NO. 04168929 REV A1
		SCALE	DO NOT SCALE DRAWING	MATERIAL
			SH 1 OF 1	


NOTE: ASSEMBLY NUMBER
U1
U1
U2
R12
R1
R2
R3
R4
R5
R6
R7
C3
U8
U9
R11
U7
U7
SONY ASSY 8516929
UNIV. LOGIC

REVISIONS					
REV	DESCRIPTION	SER. NO.	ECO NO	DATE	APP. BY
A	RELEASED TO RECORDS.			2/28/81	
A1	PROTO EVALUATION (128-81)		NFC	1/3/81	



ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

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8132 SM1208
8152 SM1279

USED ON | NEXT ASSY
APPLICATION

DRAWN R.S. 2/81 DATE
CHECK DATE
ELECT. DATE
MECH. DATE
QA DATE

SCALE 2:1
DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMAL TOLERANCE
.X
.XX
.XXX
ANGLES ±

SH 1 OF 1

SYSTRON DONNER
CORPORATION
CONCORD, CALIFORNIA

CODE IDENT 52542

MATERIAL

UNIV LOGIC P.C. ASSY (CONTROL LOGIC)

DRAWING NO.
REF | SIZE | PART NO. | REV
B | 05168929 | A

ITEM NO.	SIZE	PART NUMBER	DESCRIPTION	REFERENCE NO.	ASSY QTY	ACT. CODE	ISS. QTY	SHT QTY
1	B	05168929	P.C. ASS'Y, CONTROL LOGIC		X			
2			SCHEMATIC	7C05168929	R.			
3	B	051689	P.C. BOARD		1			
4			P.C. BOARD A/W	2D051689	R.			
5			WIRE LIST	A05168929	R.			
6		100865	EXTRACTOR		2			
8		101313	INDUCTOR, R45-4	L1	1			
9		100183	CAPACITOR, 39μF, 10V	C1	1			
11		100103	CAPACITOR, 0.01μF	C2	2			
12		100076	↓, 0.001μF	C3	1			
13		103715	↓, 10μF, 10V	C4	1			
14			↓ S/A C2	C5	1			
16		100385	DIODE, 1N4151	CR1	3			
17			↓, S/A CR1	CR2				
18			↓, S/A CR1	CR3				
21		101347	TRANSISTOR, 2N2222	Q1	2			
22			↓, S/A Q1	Q2				
25		101570	RESISTOR, 10K, ¼W, 5%	R1	9			
26			↓, S/A R1	R2				
27			↓, S/A R1	R3				
28			↓, S/A R1	R4				
29			↓, S/A R1	R5				
30		101595	↓, 8.2K, ¼W, 5%	R6	2			
31			↓, S/A R1	R7				
32		101668	↓, 180Ω, ¼W, 5%	R8	1			
33			↓, S/A R1	R9				

REVISIONS REV	DESCRIPTION
A	REL. TO RECORDS 8-25-81
A1	PROTO EVALUATION ECR 128-81 DFC 8/31-81

MODEL	JOB NO.	LOT QTY	LOT NO.	CODE IDENT
				52542

PLANNER | PREP DATE R.S. 8/7/81 | CHK'D | APP'D | MAT. DUE | B/U REQ. | B/U COMP

SYSTRON DONNER CORPORATION

CONTROL LOGIC
P.C. ASS'Y P/L

DRAWING NO.

REF	SIZE	PART NO.	REV
—	P	05168929	A1

8132S/N1208
8152S/N1279
USED ON

SHEET OF 2

FORM E8-A 11 JUL 75

ITEM NO.	SIZE	PART NUMBER	DESCRIPTION	REFERENCE NO.	ASSY QTY	ACT. CODE	ISS. QTY	SHT QTY
34			RESISTOR, S/A R1	R10				
35		101542	, 270Ω, 1/4W, 5%	R11	2			
36			, S/A R11	R12				
37		101536	, 330Ω, 1/4W, 5%	R13	1			
38			, S/A R6	R14				
39			, S/A R1	R15				
40		103349	I.C. SOCKET, 14 PIN	XU1	9			
41			, S/A XU1	XU2				
42			,	XU4				
43			,	XU5				
44			,	XU7				
45			,	XU8				
46			,	XU9				
47			,	XU10				
48			,	XU11				
51		103132	INT. CKT., 74LS74	U1	2			
52		019716	, 846	U2	1			
53			, S/A U1	U4				
54		019705	, 7400	U5	1			
55		025734	, 1808	U7	2			
56		019712	, 830	U8	1			
57		025779	, 7404	U9	1			
58			, S/A U7	U10				
59		103093	, 7408	U11	1			
62			JUMPER, #24 AWG BARE WIRE		A/R			
63			" , #30 AWG INSUL. WIRE		A/R			

REVISIONS DESCRIPTION	REV

MODEL	JOB NO.	LOT QTY	LOT NO.	CODE IDENT
				52542

PLANNER	PREP DATE	SYSTRON DONNER CORPORATION
	R.S. 8/7/81	
	CHK'D	P.C. ASS'Y P/L
MAT. DUE	APP'D	
B/U REQ.		
B/U COMP	USED ON	

DRAWING NO.			
REF	SIZE	PART NO.	REV
—	P	05168929	AL

SHEET 2 OF 2

FORM E8-A 11 JUL 75

CIRCUIT DESCRIPTION
TIME DATA CHARACTER SERIALIZER
SCHEMATIC #7-05154805-08

1. GENERAL

This card accepts time data in bcd days through seconds or bcd hours through seconds, stores these data and provides a character serial, bit parallel output in ASCII under control of external time enable and step inputs. It automatically inserts the appropriate zone bits and formatting characters.

Four different configurations can be jumper programmed on the card:

1. Assembly #05154805: the basic configuration accepts bcd days through seconds and outputs DDD:HHH:MMM:SSS CRLF most significant digit of days first. (CR and LF are carriage return and line feed characters, respectively.)

2. Assembly #05254806: accepts bcd days through seconds and outputs DDD:HH:MM:SS.SSS CRLF. (The three digits of milliseconds are inserted from a separate card.)

3. Assembly #05154807: accepts bcd hours through seconds and outputs HH:MM:SS CRLF.

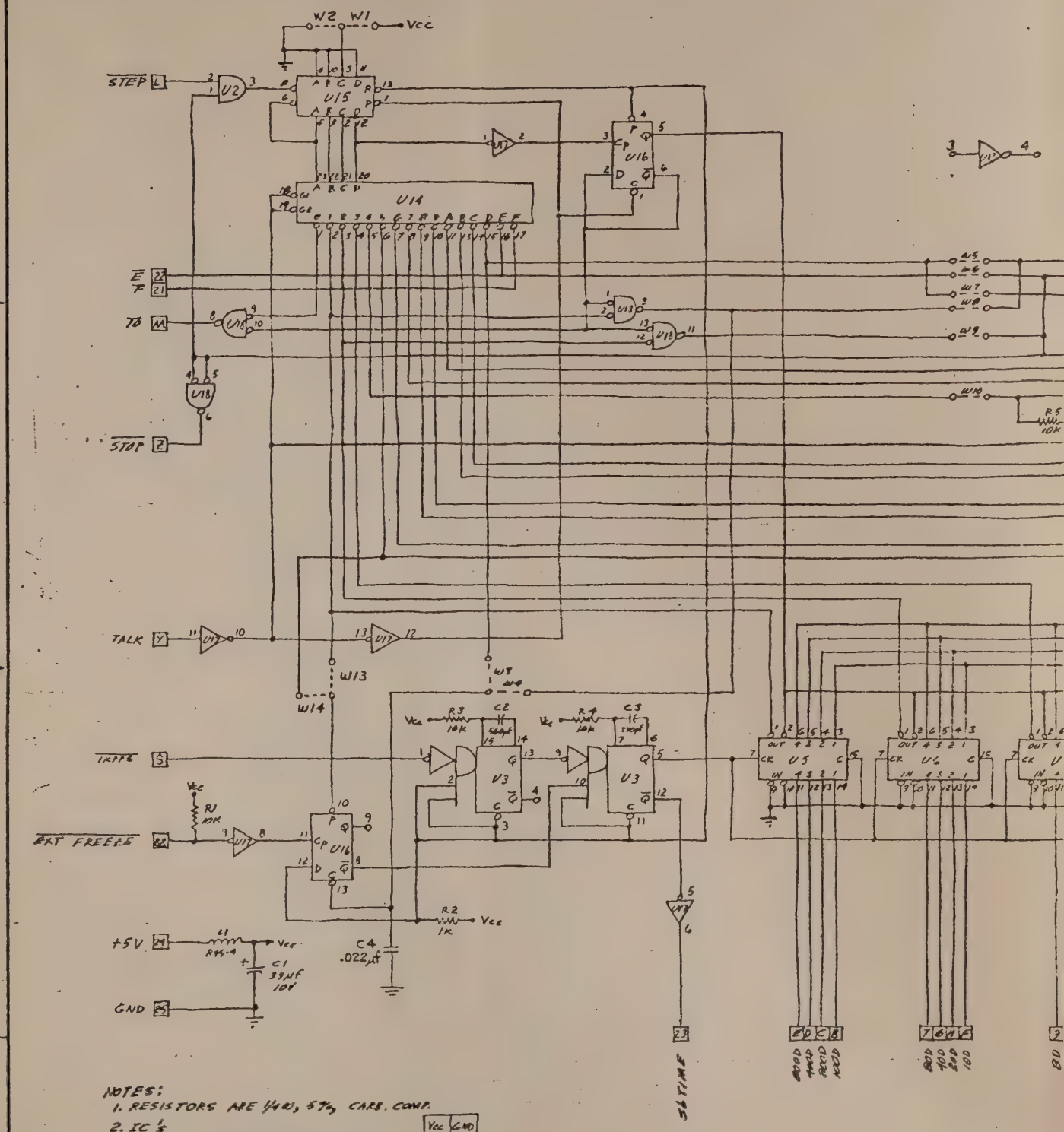
4. Assembly #05154808: also accepts bcd hours through seconds and outputs HH:MM:SS.SSS CRLF.

2. CIRCUIT DESCRIPTION

Referring to the schematic, time data from the Accumulator are loaded into the register formed from U5 through U13 by a strobe (Sb) signal which occurs each millisecond during normal operation. This signal, from one-shot U3-5, is delayed $\approx 2\ \mu s$ (by one-shot U3-13) relative to accumulator update to provide time for the data to settle. This one shot is triggered by the 1 kpps input to pin S.

When data are to be output, the time enable input to pin Y goes high and stays high during the entire sequence. This signal enables decoder U14, counter U15, U16-5 and output driver U4. The first step input to pin L sets flip-flop Ul6-9, freezing the data in the register and selects the first character for output. Subsequent step inputs feed the remaining characters out in order until the programmed end of the sequence is reached. At this point the counter is locked by closing gate U2-3 and time stop is output through pin Z. This signal terminates the time enable signal through external circuits. Flip-flop U16-9 is cleared and the data freeze terminated when the last time character in the sequence is output. The zone bits, colon, decimal point, carriage return, and line feed characters are produced by gates on U1, U2 and U18.

A mask input to pin CC is used to disable U4 when milliseconds are being selected from a separate card. The Sb time signal (pin 23) and three select signals (E, F, 10 on pins 22, 21, AA) are output for the selection of milliseconds.



NOTES:

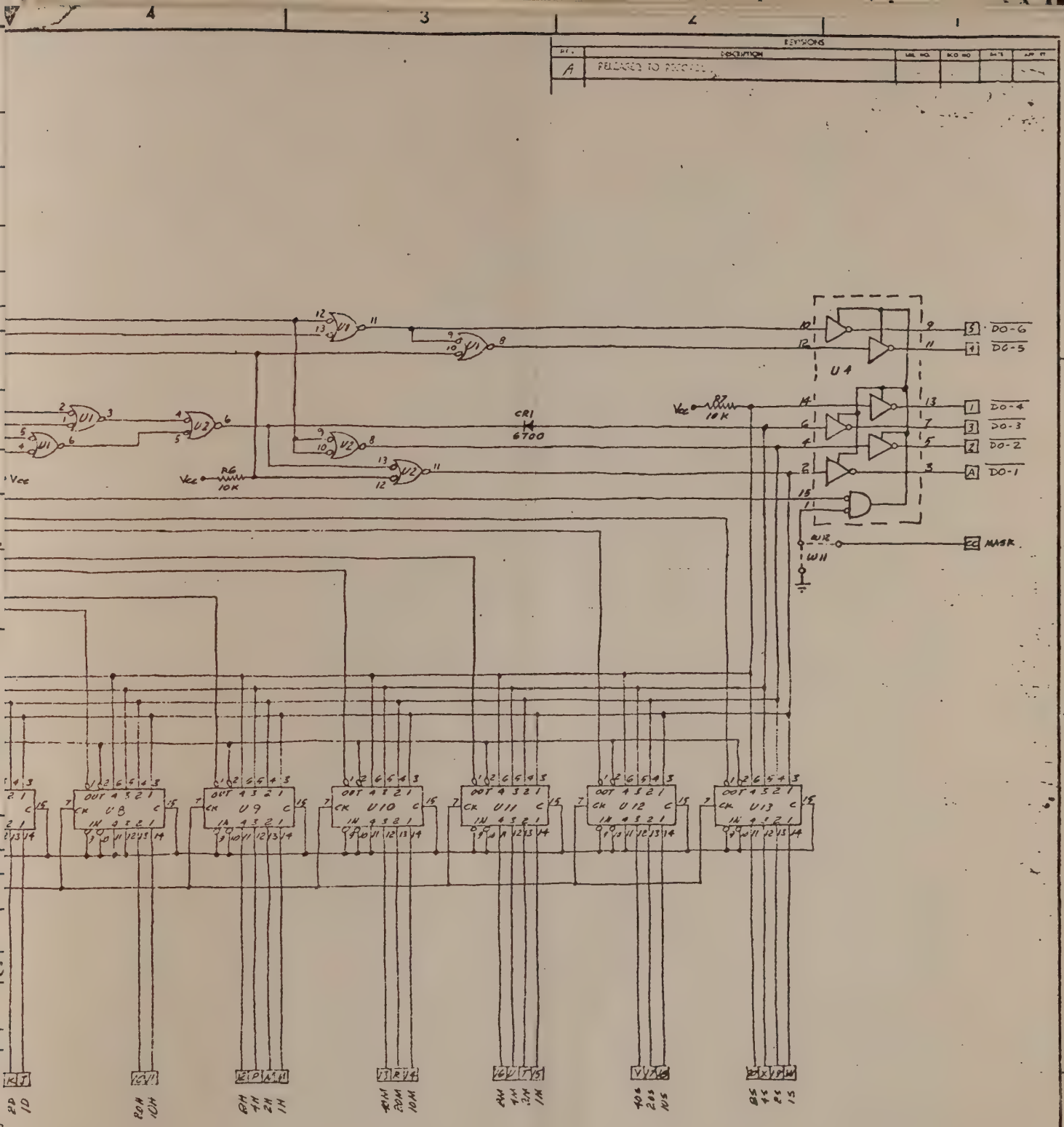
1. RESISTORS ARE 1/4 W, 5% CARB. COMP.

2. IC's

		Vcc	GND
U1, U2	MC1806 P	14	7
U3	SN74LS123 N	16	8
U4	SN74LS366AN	16	8
U5, 6, 7, 8, 9, 10, 11, 12, 13	SN74LS73 N	14	8
U14	SN74154N	24	12
U15	SN74LS197N	14	7
U16	SN74LS74AN	14	7
U17	SN74LS04N	14	7
U18	SN74LS32N	14	7

3. JUMPER PROGRAMMING

		FORMAT 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17	ASSEMBLY
DAYS → SECONDS	W2, W3, W5, W6, W10, W11, W13	DDD : HH : MM : SS SCRIB	05151805
DAYS → MILLISECONDS	W2, W4, W7, W8, W9, W10, W12, W13	DDD : HH : MM : SS . SS SCRIB	05151806
HOURS → SECONDS	W1, W3, W5, W6, W11, W14	HH : MM : SS SCRIB	05151807
HOURS → MILLISECONDS	W1, W4, W7, W8, W9, W12, W14	HH : MM : SS . SS SCRIB	05151808



ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF NO.

LIST OF MATERIALS

PROPRIETARY DATA

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DRAWN	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE X ± .XX ± ANGLES ±
CHECK	DATE	
ELECT	DATE	
MECH	DATE	
PROJ ENG	DATE	
QA	DATE	
USED ON	NEXT ASSY	
APPLICATION		
SCALE	DO NOT SCALE DRAWING	SH 1 OF 1

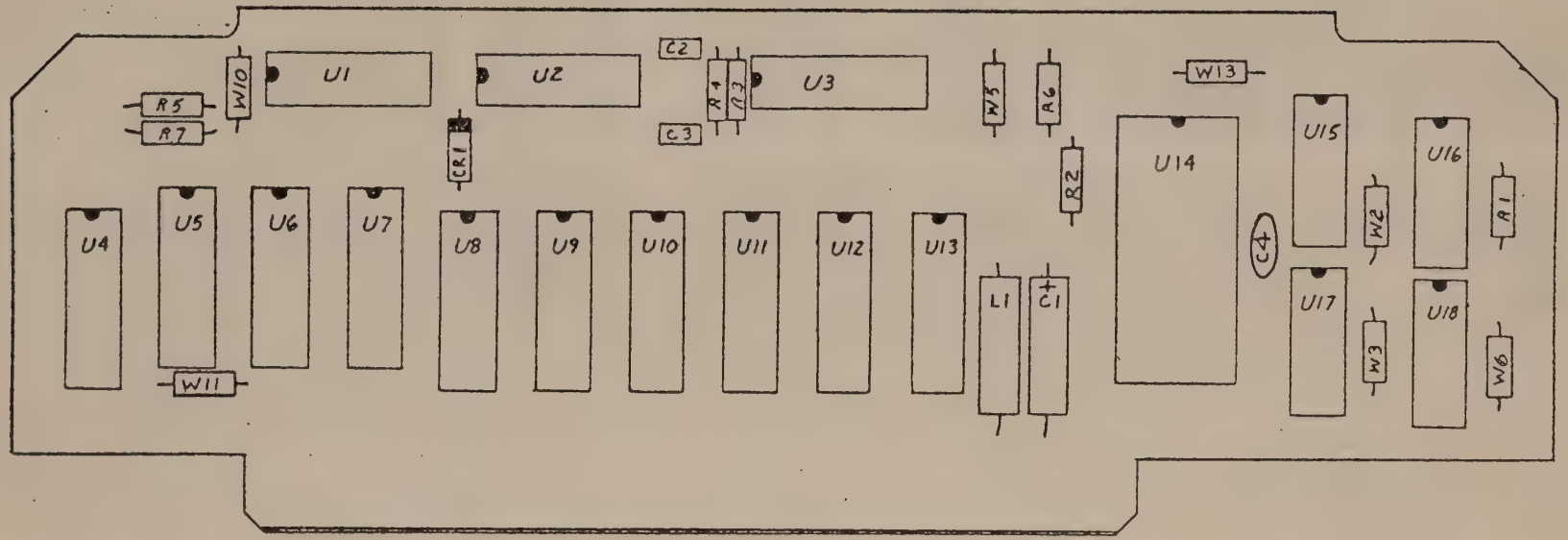
SYSTRON DONNER CORPORATION
CONCORD CALIFORNIA
CODE IDENT. 52542

TIME DATA CHARACTER SERIALIZER (DAYS → SECONDS)

MATERIAL

DRAWING NO.			
REF	SIZE	PART NO	REV
7	D	05154805	A

A	RELEASED TO RECORDS	—	-	
A1	R2 WAS 10K.		MC	8-2



LIST OF MATERIALS

CORPORATION
CONCORD CALIFORNIA

CODE IDENT 52542

PC ASSY
CH. SERIAL-
12ER

B 05154801

PARTS LIST

TIME DATA CHARACTER SERIALIZER PCB ASSEMBLY

#05154805 Rev A2

REFERENCE	DESCRIPTION	SD PART NO.
	Schematic	7-05154805
	Assembly	05154805
C1	Capacitor, 39 μF	100183
C2	Capacitor, 560 pF	117677
C3	Capacitor, 220 μF 10 V	117633
C4	Capacitor, 0.022 μF	106483
CR1	Diode, 6700	006700
L1	Inductor, R45-4	101313
R1	Resistor, 10 kΩ 5%, 1/4 W	101570
R2	Resistor, 1 kΩ 5%, 1/4 W	101569
R3 thru R7	Same as R1	
U1	Integrated Circuit, MC1806P	025733
U2	Same as U1	
U3	Integrated Circuit, SN74LS123N	103976
U4	Integrated Circuit, SN74LS366AN	118702
U5 thru U13	Integrated Circuit, SN74LS173N	118699
U14	Integrated Circuit, SN74154N	106640
U15	Integrated Circuit, SN74LS197N	103165
U16	Integrated Circuit, SN74LS74AN	103132
U17	Integrated Circuit, SN74LS04N	103749
U18	Integrated Circuit, SN74LS32N	103972
W2	Jumper Molded	102879
W3	Same as W2	
W6	Same as W2	
W10	Same as W2	
W11	Same as W2	
W13	Same as W2	

CIRCUIT DESCRIPTION
TIME REGISTER AND COMPARATOR ASSEMBLY
#7-05155801 REV B_1

1. GENERAL

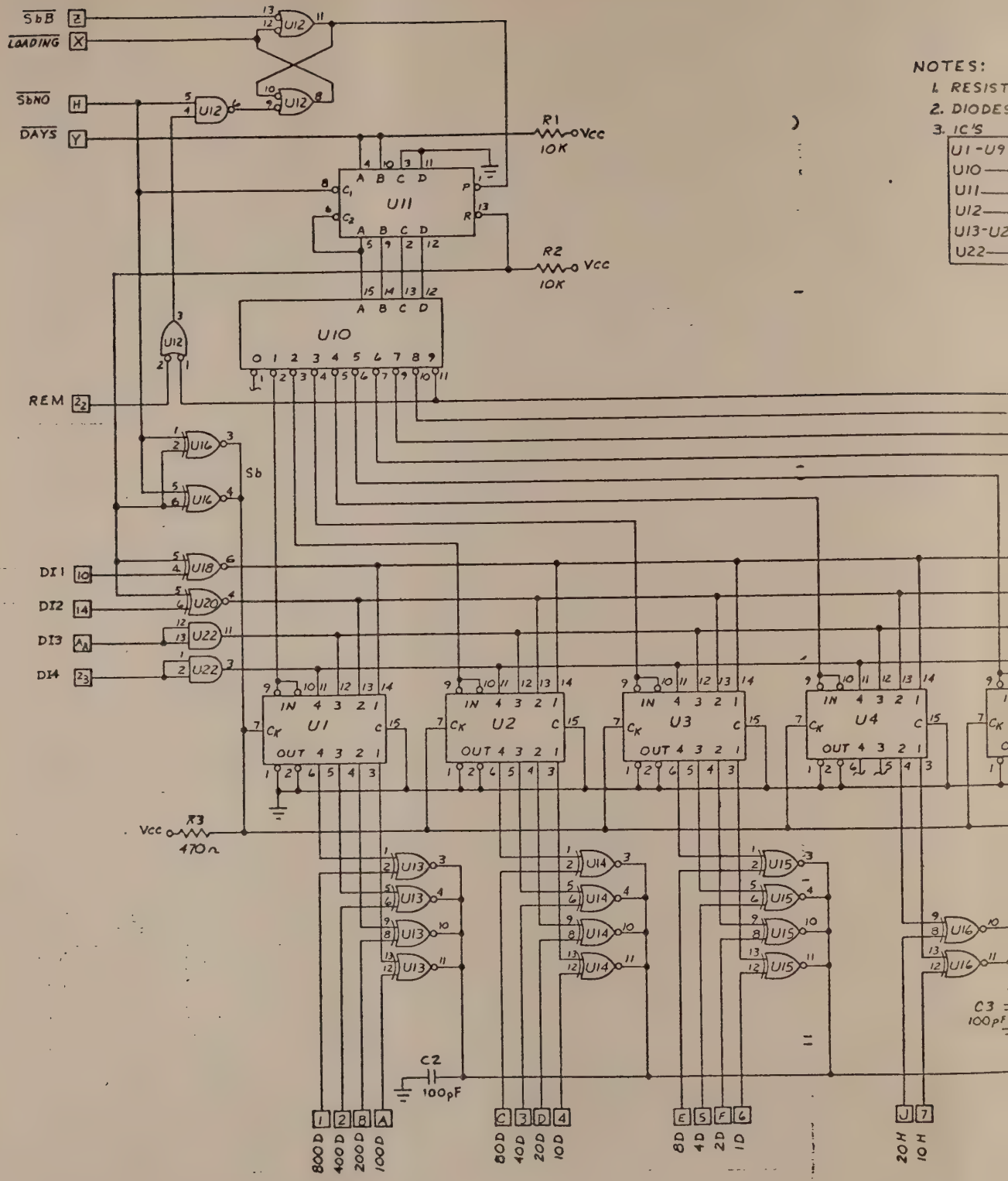
This card accepts and stores bcd time data as nine serial digits of days through seconds (or as six serial digits of hours through seconds) and compares the stored time in two groups (days and TOD) with a separate set of parallel, bcd time data inputs.

2. CIRCUIT DESCRIPTION

Referring to the Schematic, the input bits (DI 1 - DI 4) are fed through buffers on U18, U20 and U22 to the data inputs to registers U1 through U9. Each digit is steered to the proper register by the circuit shown at the upper left on the Schematic. This circuit is enabled by the $\overline{SbB}$ input to pin Z which sets flip-flop U12-11, 8 removing the preset to counter U11. This enables U11 to count SbNo pulses (pin H) provided REM input to pin 22 is high. Counter U11 will begin from a count of zero or three depending on the state of the $\overline{DAYS}$ input to pin Y. The bcd outputs from U11 are decoded by U10 and fed to registers U1 through U9.

When the last digit fills the register, U10-11 goes low enabling the reset of flip-flop U12-11, 8 through U12-3 and U12-6 thus terminating the load sequence.

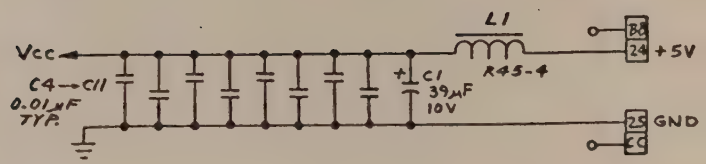
The parallel outputs from the register are compared in two groups with the parallel inputs present on the pins shown at the bottom of the Schematic. This is done in open collector exclusive NOR gates on U13 through U21. The TOD and Days coincidence signals are output through gates U22-6 and U22-8, respectively.

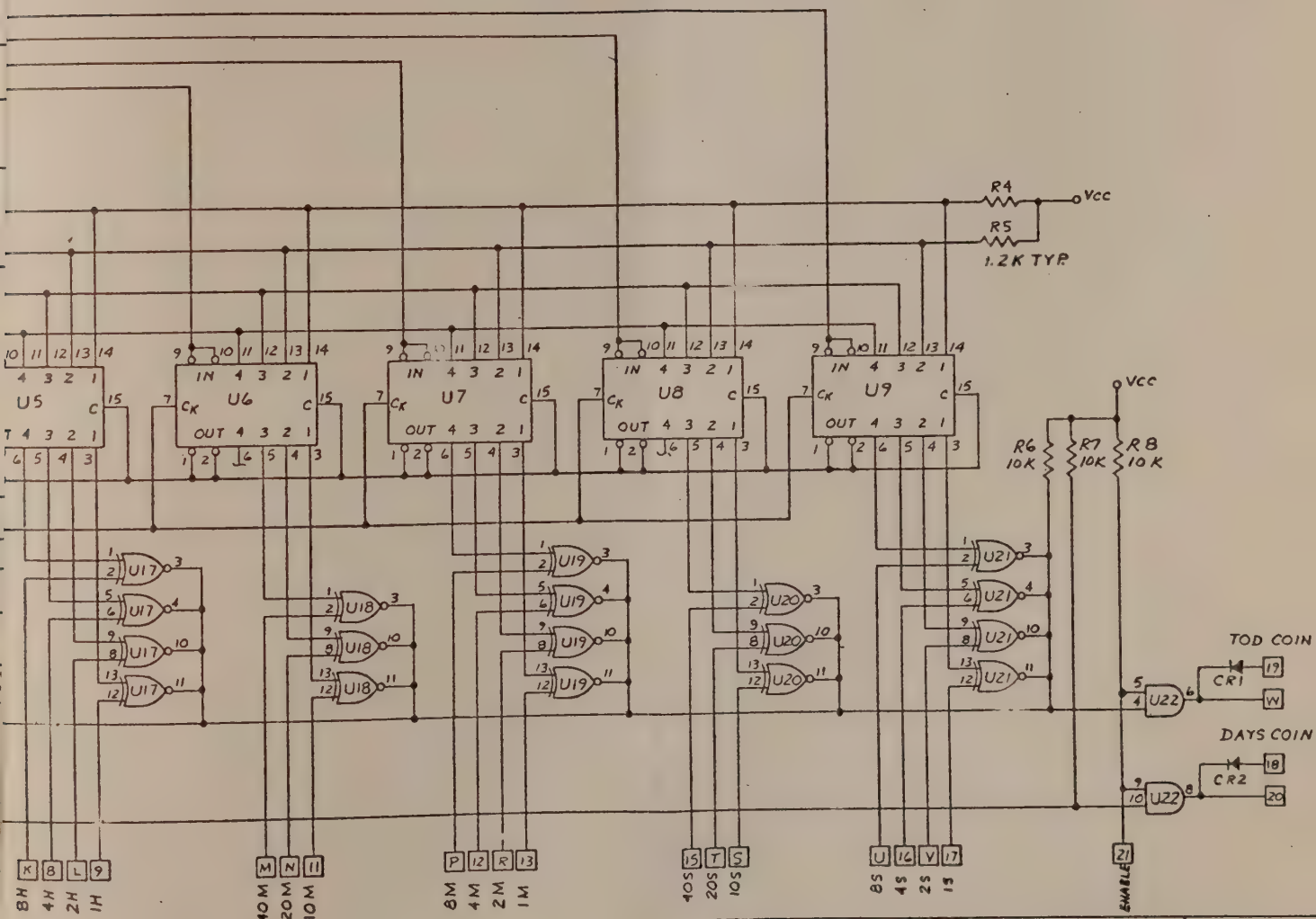

NOTES:
1. RESIST
2. DIODES
3. IC'S
U1-U9
U10
U11
U12
U13-U2
U22
SbB
LOADING
SbNO
DAYS
REM
Sb
DI1
DI2
DI3
DI4
R1
10K
R2
10K
R3
470Ω
Vcc
U10
U11
U1
U2
U3
U4
C2
100pF
C3
100pF
800D
400D
200D
100D
80D
40D
20D
10D
8D
4D
2D
1D
20H
10H

REVISIONS					
REV	DESCRIPTION	ENG NO	ECO NO	DATE	APP BY
A	RELEASED TO RECORDS				
B	PER ECO -		17525		
B1	U16 PINS 4 & 6 SWAPPED/RE TCO 1201 & ECO 17611		NFC		

RS ARE 1/8W, 5%, CARB. COMP.
ARE IN4151.

	Vcc	GND
74LS173	16	8
74LS42	16	8
74LS196	14	7
74LS00	14	7
74LS266	14	7
74LS08	14	7





ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

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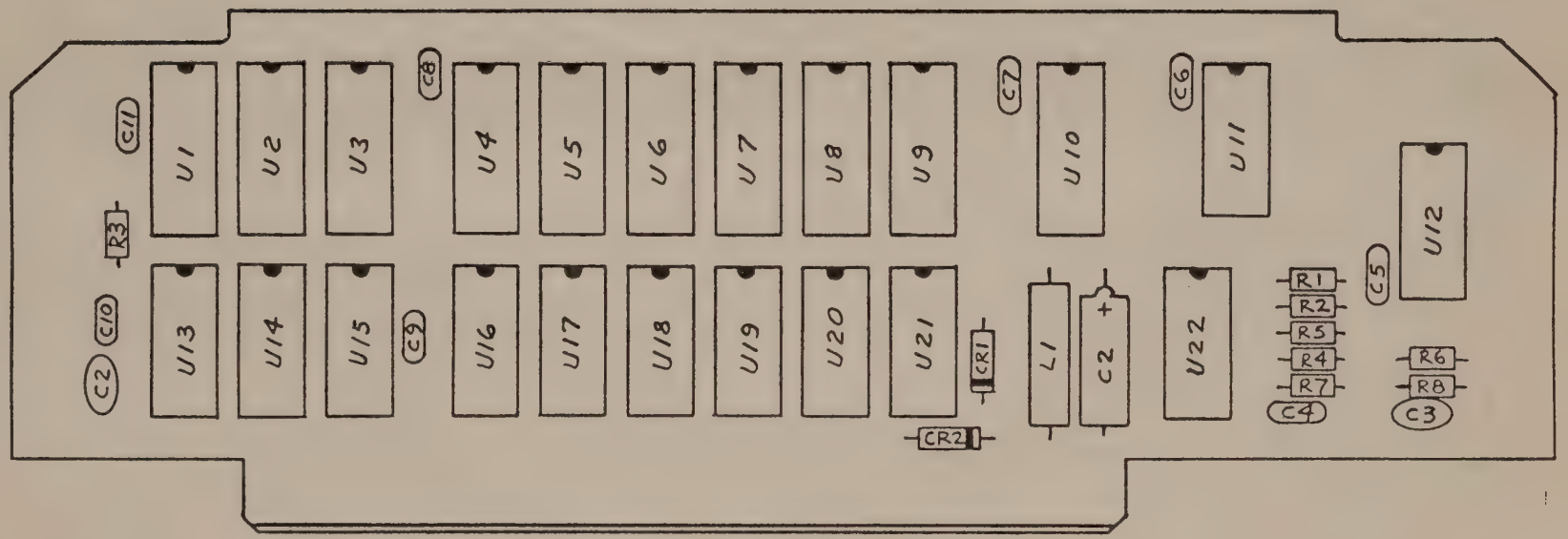
DRAWN LK	DATE 5-27-82	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
CHECK [illegible]	DATE 6-4-82	DECIMAL TOLERANCE
ELECT.	DATE	.X
MECH.	DATE	.XX
PROJECT	DATE	.XXX
QA	DATE	ANGLES ±
8152 S/N		
USED ON	NEXT ASSY	SCALE
APPLICATION		DO NOT SCALE DRAWING
		SH 1 OF 1

SYSTRON DONNER CORPORATION
CONCORD, CALIFORNIA
CODE IDENT. 52542

TIME REGISTER & COMPARATOR

MATERIAL

DRAWING NO. REF	SIZE	PART NO.	R
7	D	05155801	D



LIST OF MATERIALS

SYSTRON DONNER CORPORATION
CONCORD CALIFORNIA
CODE IDENT 52542

P.C. ASSY.
TIME REGISTER
& COMPARATOR

DRAWING NO
B 051558 01 B

SCALE 2:1

PARTS LIST
TIME REGISTER & COMPARATOR #05155801 REV B

REF.	DESCRIPTION	SD PART NO.
	Assembly	05155801
	Schematic	7-05155801
C1	Capacitor, 39 µF	100183
C2,3	Capacitor, 100 pF	117628
C4,5,6,7,8,9, 10,11	Capacitor, .01 µF, Cer. Dp.	117570
CR1,CR2	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
R1,2,6,7,8	Resistor, 10 k, 1/8 W	101697
R3	Resistor, 470 Ω, 1/8 W	101709
R4,5	Resistor, 1.2 k, 1/8 W	101969
U1,2,3,4,5,6,7, 8,9	Integrated Ckt., 74LS173	118699
U10	Integrated Ckt., 74LS42	103131
U11	Integrated Ckt., 74LS196	103164
U12	Integrated Ckt., 74LS00	103130
U13,14,15,16,17 18,19,20,21	Integrated Ckt., 74LS266	117378
U22	Integrated Ckt., 74LS08	103967
	Extractor	100865

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